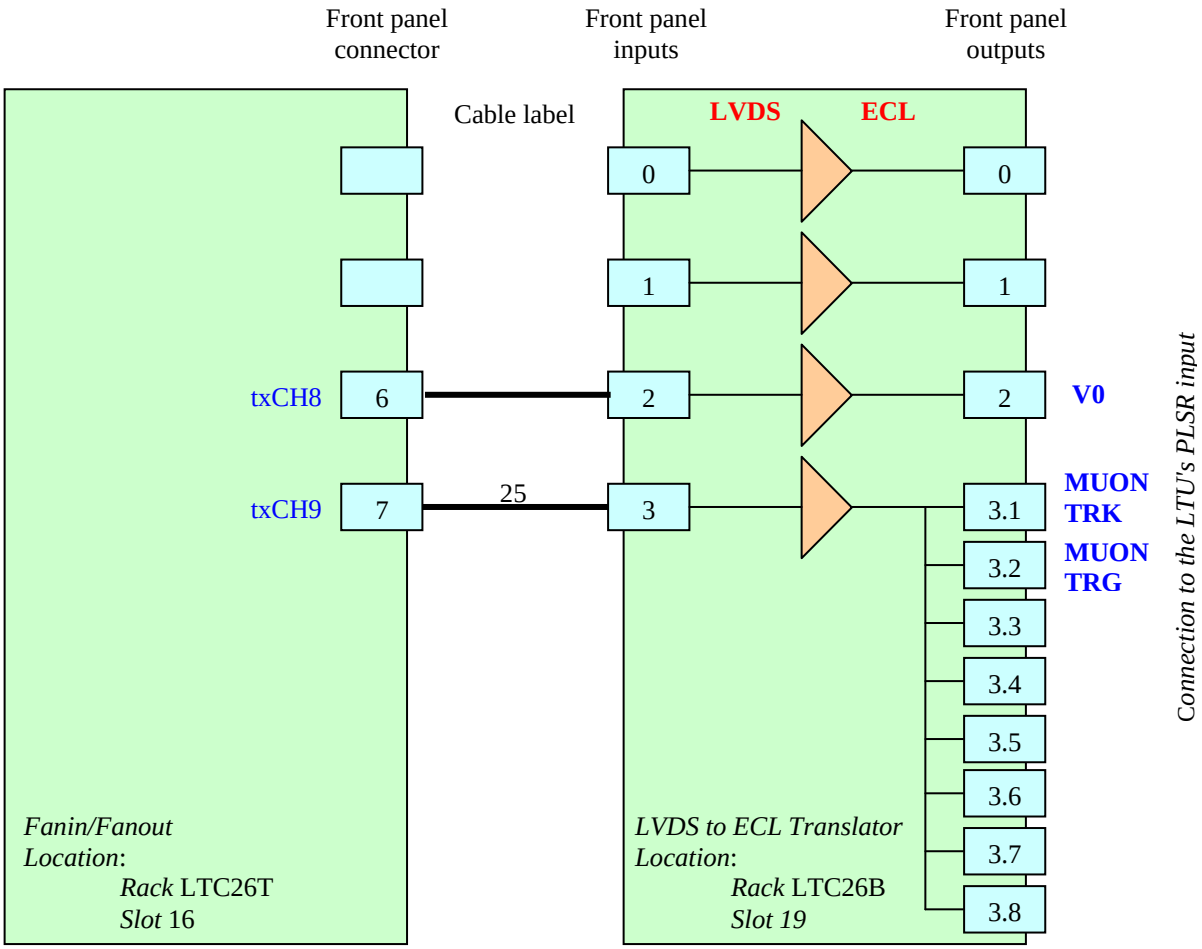
File: ltu_pulser3.doc
Last updated: 14 August 2009

L0 Trigger signal connection to the LTU's *Pulser* input (PLSR)

(Third LVDS-ECL module from right)



Board designed by M. Krivda and F. Formenti
Part of the Trigger Multiplexer

Board designed by Michel Morel, SPD group