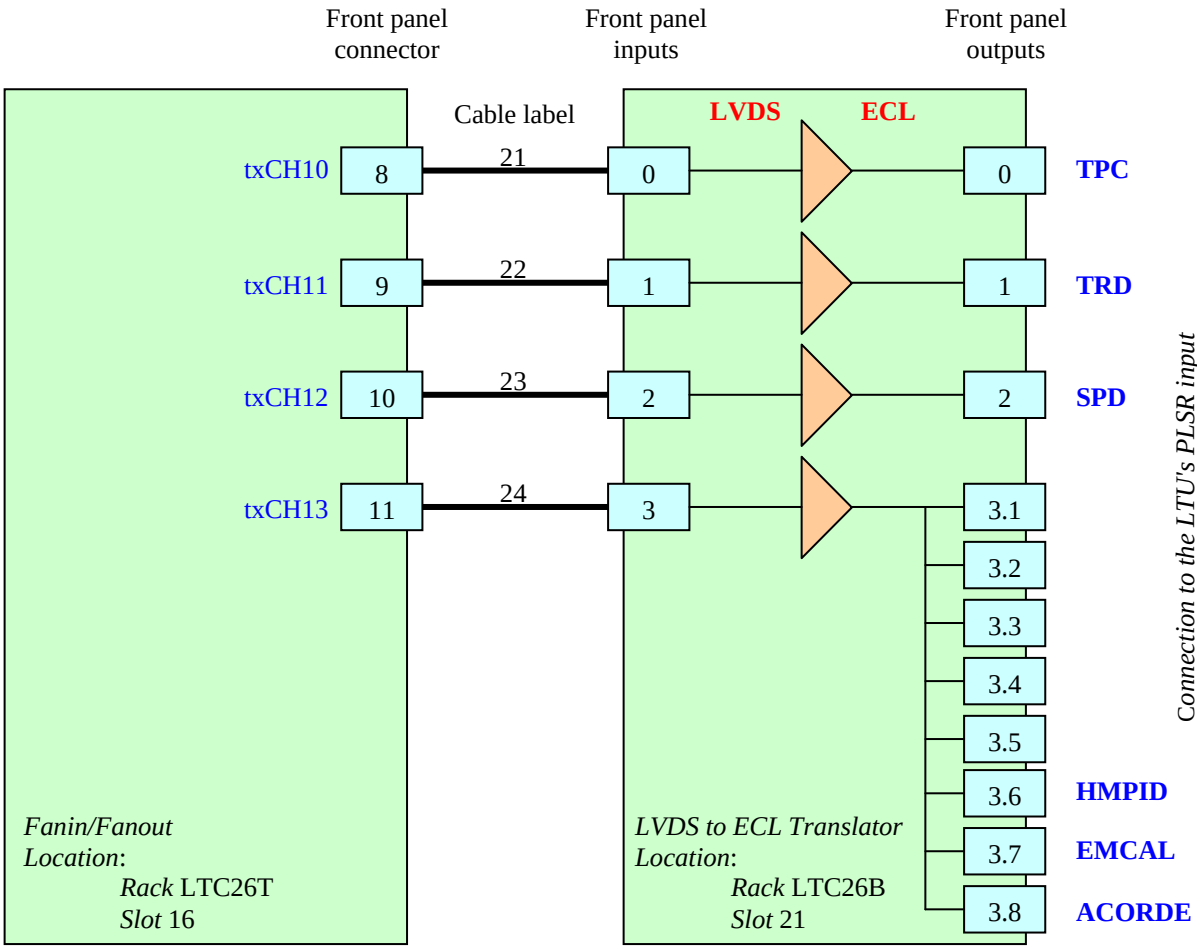
File: ltu_pulser1.doc
Last updated: 1 July 2009

L0 Trigger signal connection to the LTU's *Pulser* input (PLSR)

(First LVDS-ECL module from right)



Board designed by M. Krivda and F. Formenti
Part of the Trigger Multiplexer

Board designed by Michel Morel, SPD group