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Implementation of the rare-event handling logic - proposal

Introduction

A comprehensive review of the rare-event handling in ALICE is coming to a conclusion: a proposal was presented to the Technical Board (TB) on 26 November 2002 and the final approval is expected in the next meeting, on 16 December 2002.

"Early history" and the corresponding references are available on the Central Trigger Processor (CTP) web site [1]; more recent presentations, containing essential simulation results [2][3], are filed as TB documents. This proposal "translates" the conclusions concerning the hardware implementation into the language of the CTP requirements; when approved, the text shall be appended to the CTP URD [4].

Hardware requirements

1. An additional veto option, **All/Rare** (**A/R**), shall be added to the **L0** class-trigger logic (**Figure 1**) and included in the trigger-class definition. When the option is selected, the corresponding trigger class could become active only if the **A/R** control bit is asserted.

Note 1: In normal operation, the veto would be used for *all the classes that are not associated with rare events*.

2. The **A/R** signal shall be generated by the CTP processor, *but the timing and the status of the signal shall be fully controlled by the DAQ system*.

Note 2: The appropriate DAQ-CTP communication protocol is to be defined.

3. The asserted status (*"all classes enabled"*) shall be a default state for the **A/R** signal.

4. If required, the monitoring (timing) of the signal shall be performed by the CTP control processor.

Note 3: The expected switching rate of the **A/R** signal is low. Typical example [2]: *all* state - 1second; *rare only* state - 8 seconds.

References:

[1] ALICE CTP web site: (ALICE-Projects-Trigger), or, directly, http://www.ep.ph.bham.ac.uk/user/pedja/alice/.

[2] T. Antičić *et al*., *Trigger and DAQ system simulation,* presentation to the ALICE TB on 26 November 2002.

[3] T. Antičić, *Maximizing acceptance of rare/interesting events,* presentation to the ALICE TB on 26 November 2002.

[4] *ALICE Central Trigger Processor: User Requirement Document,* current version available on the ALICE CTP web site [1].

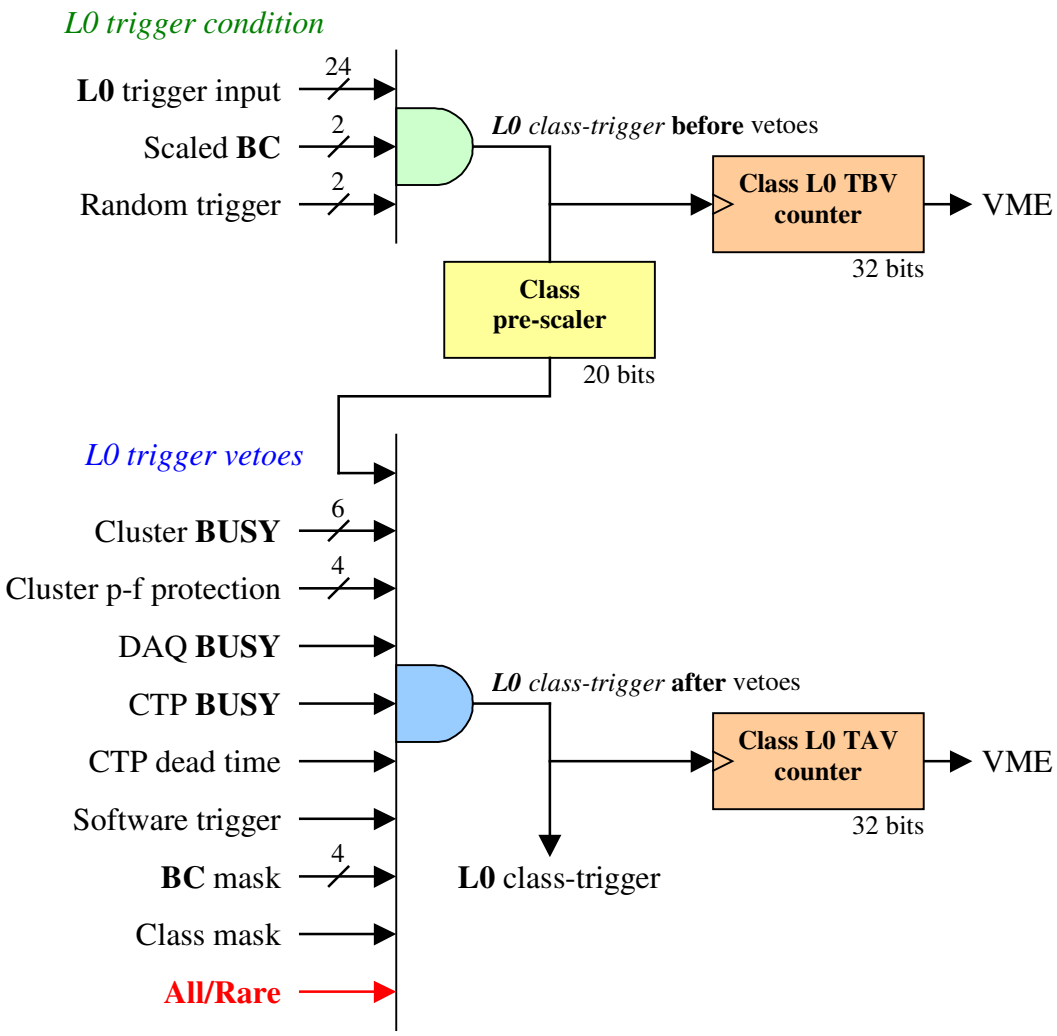

Figure 1 **L0** class-trigger logic