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LTUvi - Software Model Update

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The VME address map of the *LTUvi* board

Address	Mnemonic	Description	Wr	Rd	Section
		***VME Controller* FPGA**			
H"**01**"	CODE_ADD	LTU *Board Type* code		+	**3.2.1**
H"**02**"	SERIAL_NUMBER	LTU board *Serial Number*		+	**3.2.2**
H"**03**"	VERSION_ADD	*VME controller FPGA Firmware Version*		+	**3.2.3**
H"**0A**"	SOFT_RESET	LTU software reset (dummy data)	+		**3.2.1**
H"**10**"	FLASHACCESS_INCR	Flash memory access with add. increment	+	+	**3.5**
H"**11**"	FLASHACCESS_NOINCR	Flash memory access, no add. increment	+	+	**3.5**
H"**12**"	FLASHADD_CLEAR	Clear *Flash Memory Address*	+		**3.5**
H"**13**"	FLASH_STATUS	*Flash memory Status* word		+	**3.5**
H"**14**"	CONFIG_STATUS	*Configuration Status* word		+	**3.6.1**
H"**15**"	CONFIG_START	*Start Configuration* command	+		**3.6.1**
H"**16**"	TEMP_START	*Start Temperature Read* command	+		**3.6.2**
H"**17**"	TEMP_STATUS	*Temperature Read Status*		+	**3.6.2**
H"**18**"	TEMP_READ	*Temperature Read Data*		+	**3.6.2**
H"**19**"	MASTER_MODE	Master write destination (TTCvi or LTU)	+	+	**3.6.3**
		***LTU Logic* FPGA**			
H"**20**"	VERSION_ADD	*LTU logic FPGA Firmware Version*		+	**3.2.3**
H"**31**"	BC_STATUS	*BC Status* word		+	**M.1**
H"**33**"	ADC_START	*ADC Start* command (dummy data)	+		**3.7.1**
H"**34**"	ADC_DATA	*ADC Data* (including **ADC BUSY** status)		+	**3.7.1**
H"**35**"	ERROR_ENABLE	*Enable Error Emulation* command	+		**3.15**
H"**36**"	ERROR_STATUS	*Error Emulation Status* word		+	**3.15**
H"**37**"	ERROR_SELECTOR	Error selector (*Set Error* mode)	+		**3.15**
H"**38**"	ERROR_DEMAND	*Error on Demand* request	+		**3.15**
H"**3A**"	ORBIT_CLEAR	Clear emulator's **ORBIT** counter	+		**3.13**
H"**3B**"	EMULATION_START	*Start Emulation* command (dummy data)	+		**3.13**
H"**3C**"	QUIT_SET	*Set QUIT* command (dummy data)	+		**3.13**
H"**3D**"	BREAK_SET	*Set BREAK* command (dummy data)	+		**3.13**
H"**45**"	SLM_ADD_CLEAR	Clear *SLM Read* and *Write Addresses*	+		**3.13**
H"**46**"	SLM_DATA	*SLM Data* word		+	**3.13**
H"**47**"	EMU_STATUS	*Emulator BUSY* status		+	**3.13**
H"**49**"	SOFT_TRIGGER	Software generated **START**	+		**3.14**
H"**4E**"	BUSY_ENABLE	**BUSY 1/BUSY2** input enable	+		**3.10**
H"**4F**"	BYSY_STATUS	**BUSY** status word		+	**3.10**
H"**50**"	SOFT_BUSY	Software generated **BUSY**	+		**3.10**
H"**52**"	L1MAX_CLEAR	Clear *L1 FIFO Maximum Occupancy*	+		**3.11**
H"**53**"	L2MAX_CLEAR	Clear *L2 FIFO Maximum Occupancy*	+		**3.11**
H"**56**"	FIFO_MAX	*L1/L2 FIFO Maximum Occupancy*		+	**3.11**
H"**57**"	SOFT_LED	*SoftLED* option read word		+	**R.1**
H"**5A**"	BUSYMAX_DATA	*BusyProbe* option - longest BUSY time		+	**R.2**
H"**5B**"	BUSYMINI_DATA	*BusyProbe* option - shortest BUSY time		+	**R.2**
H"**5D**"	MINIMAX_CLEAR	Clear BUSYMAX/BUSYMINI counters	+		**R.2**
H"**66**"	PIPELINE_CLEAR	*Pipeline Clear* command (dummy data)	+		**3.13**
H"**67**"	SSM_COMMAND	*SSM Command* word	+		**M.3**
H"**68**"	SSM_START	*SSM Start* command (dummy data)	+		**3.17**
H"**69**"	SSM_STOP	*SSM Stop* command (dummy data)	+		**3.17**
H"**6A**"	SSM_ADDRESS	*SSM Address* word	+	+	**3.17**
H"**6B**"	SSM_DATA	*SSM Data* word	+	+	**3.17**
H"**6C**"	SSM_STATUS	*SSM Status* word		+	**M.3**
H"**6E**"	TIMING_TEST	*Timing Test* word	+		**3.19**
H"**6F**"	PLL_RESET	*PLL Reset* command (dummy data)	+		**N.1**
H"**72**"	TTC_STATUS	TTC FIFO status word		+	**N.2**

Address	Mnemonic	Description	Wr	Rd	Section
H"**75**"	COPY_COUNT	Copy counter command (dummy data)	+		**R.3**
H"**76**"	COPY_BUSY	Copy BUSY status word		+	**R.3**
H"**77**"	COPY_CLEARADD	Clear copy memory add. (dummy data)	+		**R.3**
H"**78**"	COPY_READ	Copy memory data read		+	**R.3**
H"**132**"	BC_DELAY_ADD	BC delay register (5 bits, 1ns/bit)	+	+	**3.7.2**
H"**139**"	ERROR_RATE	Error rate setting	+	+	**3.15**
H"**13E**"	LAST_BC	Number of the last BC in the LHC orbit	+	+	**3.8**
H"**13F**"	PREPULSE_BC	BC number of the **PREPULSE**	+	+	**3.8**
H"**140**"	CALIBRATION_BC	BC number of the calibration trigger	+	+	**3.8**
H"**141**"	GAP_BC	First BC of the LHC *Large Gap*	+	+	**3.8**
H"**142**"	ORBIT_BC	BC number of the emulator's **ORBIT**	+	+	**3.8**
H"**143**"	L1_DELAY	Emulator's **L0** to **L1** delay (in BCs)	+	+	**3.8**
H"**144**"	L2_DELAY	Emulator's **L0** to **L2** delay (in BCs)	+	+	**3.8**
H"**148**"	START_SET	Settings for the **START** signal	+	+	**3.14**
H"**14A**"	RANDOM_NUMBER	Rate of the *Random* **START**	+	+	**3.14**
H"**14B**"	COUNT_PERIOD	Period of the *Scaled-down BC* **START**	+	+	**3.14**
H"**14C**"	TTC_INTERFACE	Channel A/B output delay; L0 over TTC	+	+	**M.2**
H"**14D**"	MODE	Setting of *Global/Stand-alone* mode	+	+	**3.22**
H"**151**"	L1_FORMAT	Setting of the *L1 Message* format	+	+	**3.23**
H"**154**"	SCOPE_SELECT	Selection of ScopeProbe **A/B** signals	+	+	**3.18**
H"**155**"	BACKPLANE_EN	Backplane output enable	+	+	**3.12**
H"**15C**"	MINIMAX_SELECT	Select input for *MinimaxBusy* option	+	+	**R.2**
H"**15E**"	MINIMAX_LIMIT	Threshold for *LongBusy* option	+	+	**R.2**
H"**16B**"	CLEAR_COUNTER	Clear counter command	+	+	**R.3**
H"**170**"	ORBIT_TIME	Start of the ORBIT transmission	+	+	**N.2**
H"**171**"	PP_TIME	Start of the PREPULSE transmission	+	+	**N.2**
H"**172**"	TTC_DATA	TTC FIFO write data	+	+	**N.2**
H"**1FA**"	TEST_ADD	*LED Test* flag	+	+	**3.3.1**

Address is the *local address* (see section **3.1.6**).

Note: Write *and* read addresses H"**1***NN*" are read from the *SpyMemory* - the read data are correct only *after* the preceding write.

Mnemonic is the symbolic name used in the LTU FPGA firmware documentation.

Wr and **Rd** refer to the VME write and VME read access.

A very brief **Description** is expanded in the corresponding section of [1], for pointers of the type **3.7.2** and similar; or in the following sections **M.1-3**, **R.1-3** and **N.1-2.**

References:

[1] *LTU Software Model*, [6]
[2] [6], *CTP Documentation*, *List of Software Notes*
[3] *TTCrx Reference Manual*, [7]
[4] *TTCvi - MkII, TTC-VMEbus Interface*, [7]
[5] *LTU Preliminary Design Review*, [6]
[6] ALICE Trigger web site: http://epweb2.ph.bham.ac.uk/user/pedja/alice/
[7] TTC web site: http://ttc.web.cern.ch/ttc/

Introduction

The ***LTUvi*** board - the original LTU board with the version H"B0" or later of the *LTU Logic* FPGA firmware - performs *all* the logic functions required in the ALICE TTC partition; the TTCvi board is not required any longer.

The *BusyProbe* option has been added to monitor and analyse elements of sub-detector BUSY; the list of internal signals accessible *via* the *ScopeProbe* option has been modified, as well as the bit-allocation in the *SnapShot* memory; some *new* control and status words have been added; some "old" words have been either modified or removed. All the modification and additions have been documented in this note.

LTU Software Model [1] still remains the main software reference, but the updated *VME Address Map of the LTUvi Board* should be consulted first: it contains pointers (column *Section*) to the up-to-date documentation.

M Modifications of the existing words

M.1 *BC Status* word

***BC_STATUS* word, read only:**

Address: H"**31**"

Bit allocation:

Data bits	Content
D[0]	*BC Error* flag
D[1]	*PLL Locked* flag
D[2]	*ORBIT Error* flag

The *ORBIT Error* flag indicates either the absence or a wrong (too fast or too slow) frequency of the ORBIT input signal; see [1], section **3.20** for the rest of application details.

M.2 *TTC Interface* word

***TTC_INTERFACE* word, write and read:**

Address: H"**14C**"

Bit allocation:

Data bits	Content
D[0]	*Delay Channel B* flag
D[1]	*Delay Channel A* flag
D[3]	Enable *LO over TTC* option

When the *Delay* flag is asserted, the corresponding *Channel A*/*Channel B* output (LTU's connector L1/ORBIT) is delayed by a half of a BC interval (12.5ns). The option is provided in order to comply with the TTCex board *set-up time* and *hold time* requirements.

The *L0 over TTC* option is active when the *Enable* bit is *asserted*.

Note: Data bit D[2] is not used.

See [1], section **3.9** for the rest of application details.

M.3 *SnapShot* memory *Command* and *Status* words

***SSM_COMMAND* word, write only:**

Address: H"**67**"

Bit allocation:

Data bits	Content
D[4]	*Select CTP* flag
D[1]	*Operation* bit
D[0]	*Mode* bit

If the *Select CTP* flag is asserted, the CTP inputs to the LTU are connected to the data bits D[0..6] of the *SnapShot* memory, regardless of the state of the *Mode* bit; the option makes the LTU compatible with all the other trigger boards for tests of connectivity. Use of the *Operation* and the *Mode* bits is explained in [1], section **3.17**.

***SSM_STATUS* word, read only:**

Address: H"**6C**"

Bit allocation:

Data bits	Content
D[4]	*Select CTP* flag
D[2]	*SSM BUSY*
D[1]	*Operation* bit
D[0]	*Mode* bit

The *Mode*, the *Operation*, and the *Select CTP* flags are set by the *SSM_COMMAND* word; the SSM BUSY flag is controlled by the hardware.

M.3.1 *SnapShot* memory data bit allocation

Data	*Firmware notation*	*Signal*	*Description*
0	!select_ctp & ltu_select.orbit_sel # select_ctp & !/ctp_orbit	ORBIT	Selected ORBIT (1µs pulse)
1	!select_ctp & ltu_select.prepulse # select_ctp & !/ctp_prepulse	PP request	PP request (25ns pulse); includes errors
2	!select_ctp & ssh_l0 # select_ctp & !/ctp_l0	L0 output	L0 output; includes errors
3	!select_ctp & ltu_select.l1_strobe # select_ctp & !/ctp_l1	L1 STROBE	Selected L1 STROBE; includes errors
4	!select_ctp & ltu_select.l1_data # select_ctp & !/ctp_l1_data	L1 DATA	Selected L1 DATA
5	!select_ctp & ltu_select.l2_strobe # select_ctp & !/ctp_l2_strobe	L2 STROBE	Selected L2 STROBE; includes errors
6	!select_ctp & ltu_select.l2_data # select_ctp & !/ctp_l2_data	L2 DATA	Selected L2 DATA
7	ltu_busy.s_sbusy	BUSY1+BUSY2	Subdetector BUSY (BUSY1 + BUSY2)
8	ltu_busy.s_busy	BUSY	LTU internal BUSY; all constituents
9	l1fifo_wr.l1nearly_full	L1FIFO full	*L1 Message* FIFO nearly full status
10	l2fifo_wr.l2nearly_full	L2FIFO full	*L2 Message* FIFO nearly full status
11	out_l1	Channel A	TTC *Channel A* output
12	out_orbit	Channel B	TTC *Channel B* output
13	ttcvi.ttc_busy	TTC BUSY	TTC *Channel B* transmission in progress
14	ttcvi.pp_select	PP transmit	PP transmission in progress (17 BCs)
15	strobe	VME strobe	VME strobe (read or write)
16	ssh_start_all.q	START	All emulation START trigger options
17	ltu_select.any_error	Any error	Any error signal (25ns pulse)

Note: *The Select CTP* flag is set with the *SSM_COMMAND* word (see above).

R References for some of the new words

Some of the logic blocks have been used on other trigger boards; the corresponding control words have been documented elsewhere. The following sections provides the necessary references.

R.1 *Software LED* word

The *SoftLED* option is used on all the CTP boards. The option is described in the software note ***Software LEDs (SoftLED option)*** [2]; the note contains the bit allocation of the *SOFT_LED* word (address H"**57**"; read only).

R.2 *BusyProbe* option

The *BusyProbe* option is used on the BUSY boards. The option is described in the software note ***TooBUSY - a tool for monitoring of sub-detectors' BUSY response*** [2]; the note contains the bit allocation for common control and status words:

- *BUSYMAX_DATA* (address H"**5A**"; read only)
- *BUSYMINI_DATA* (address H"**5B**"; read only)
- *MINIMAX_CLEAR* (address H"**5D**"; dummy write)
- *MINIMAX _LIMIT* (address H"**15E**"; write and read)

***MINIMAX_SELECT* word, write and read:**

Address: H"**15C**"

Data bits	Content
D[2..0]	Signal selection code (0 to7):
0, 6, 7	All including LTU BUSY
1	Synchronised BUSY 1 input
2	Synchronised BUSY 2 input
3	*L1 Message* FIFO *Nearly Full* status
4	*L2 Message* FIFO *Nearly Full* status
5	Synchronised sub-detector BUSY

R.3 LTUvi counters

The implementation of the counters on the LTU board is the same as the scheme used on all the CTP boards; the logic is described in the software note ***L0 Counters*** [2]; the note contains the bit allocation for all control and status words:

- *COPY_COUNT* (address H"**75**"; dummy write)
- *COPY_BUSY* (address H"**76**"; read only)
- *COPY_CLEARADD* (address H"**77**"; dummy write)
- *COPY_READ* (address H"**78**"; read only)
- *CLEAR_COUNTER* (address H"**16B**"; write and read)

R.3.1 List of LTUvi counters; address allocation in *CounterCopy* memory

Time counters **(Table 1)**

Resolution: 0.4µs

Address	*Firmware notation*	*Signal*	*Description*
0	VCC	Time	Elapsed time
1	s_in_busy1	BUSY1 input	Synchronised BUSY1 input
2	s_in_busy2	BUSY2 input	Synchronised BUSY2 input
3	ltu_busy.s_sbusy	Sub-detector BUSY	Synchronised sub-detector BUSY
4	ltu_busy.s_busy	BUSY	LTU's internal BUSY; all constituents
5	l1fifo_wr.l1nearly_full	L1 FIFO full	*L1 Message* FIFO nearly full status
6	l2fifo_wr.l2nearly_full	L2 FIFO full	*L2 Message* FIFO nearly full status
7	bc_error	BC Error	Synchronised *BC Error* status

Table 1 LTUvi *time* counters - *CounterCopy* memory allocation

Note: *"Elapsed time"* timer (address 0) counts continuously; it is intended for real time measurements.

Fast-signal counters **(Table 2)**

Rate: arbitrary

Address	*Firmware notation*	*Signal*	*Description*
8	emu_start.start_all	START	Selected emulation START trigger
9	ltu_busy.s_busy	BUSY pulse	LTU's internal BUSY transition (25ns)
10	l1fifo_wr.l1nearly_full	L1 FIFO pulse	*L1 Message* FIFO full transition (25ns)
11	l2fifo_wr.l2nearly_full	L2 FIFO pulse	*L2 Message* FIFO full transition (25ns)
12	ltu_select.any_error	ANY ERROR	ANY ERROR pulse (25ns)
13	bc_error	BC Error pulse	*BC Error* status transition (25ns)
14	minimax.busy_long	Long BUSY	BUSY over threshold (*BusyProbe*, 25ns)

Table 2 LTUvi *fast-signal* counters - *CounterCopy* memory allocation

Slow-signal counters **(Table 3)**

Rate: maximum 1 count *per* 4µs

Address	*Firmware notation*	*Signal*	*Description*
15	ltu_select.prepulse	PP Request	PP Request (25ns); includes errors
16	ltu_select.l0	L0	L0 output; includes errors
17	ltu_select.l1_only	L1 only	Selected L1 (25ns); includes errors
18	ltu_select.l1_strobe	L1 STROBE	Selected L1 STROBE (25ns); includes errors
19		L2a	L2a strobe (25ns); includes errors
20		L2r	L2r strobe (25ns); includes errors

Table 3 LTUvi *slow-signal* counters - *CounterCopy* memory allocation

N Definition of new LTUvi words

N.1 *Reset FPGA Phase Locked Loop* command

PLL_RESET **word, dummy write:**

Address: H"**6F**"

The word resets the BC PLL in the LTU/LTUvi Logic FPGA.

N.2 TTCvi emulation logic

N.2.1 General

In the original ALICE TTC partitions, the TTCvi board had been used to control data transmission over the *Channel B*; the data had been written from the LTU board

acting as a VME master; or from the VME processor. The *Channel A* transmission had been fully controlled by the LTU board.

In the *LTUvi* version, the generation of the *Channel B* serial data stream has been "imported" into the LTU; the TTCvi board is no longer required. The LTUvi board is no longer a *VME master* - the internal *Device Wants Bus* (DWB) signal is permanently cleared.

In order to make the "transition" as transparent to the software as practical, the TTCvi's approach, the conventions, the word formats, *etc*. have all been preserved as fully as possible; all the new LTUvi words that are used to control the TTCvi emulator logic are described in the following sections.

The TTC *Channel B* is used to transmit the following data streams:

Data stream	***Frame format***	***Priority***
ORBIT	Broadcast frame	0
PREPULSE	Broadcast frame	1
L1 Message	Individually-addressed frame	2
L2 Message	Individually-addressed frame	3
VME word	Individually-addressed frame	4

The formats of the *Broadcast Frame* (16 serial bits) and of the *Individually-addressed Frame* (42 serial bits) are define in [3], Chapter 2.

The data part (8 bits; [3], Chapter 5) of the ORBIT transmission is set by the firmware to H"**FC**"; in case of the PREPULSE transmission, the data bits are H"**01**".

Priority level 0 is the highest; lower priority transmissions wait until the higher priority transmissions - in progress or pending - are completed. In order to secure undisturbed timing of the ORBIT and PREPULSE signals, the two transmissions are preceded by an *Inhibit* interval [4]; during the interval, a start of any new, lower priority transmission is prevented; the widths of the interval is fixed by the firmware to 44 BCs. A correct transmission of the ORBIT is assured by design. In order to secure a correct transmission of the PREPULSE, the requested transmission must not coincide with the ORBIT *Inhibit* interval; if it does, the PREPULSE transmission shall be abandoned. The timing of the ORBIT and the PREPULSE transmission is scheduled by software settings (*ORBIT_TIME* and *PP_TIME* words, see the following sections).

N.2.2 Transmission of ORBIT and PREPULSE

The transmission is automatic - no software intervention is required; the software only controls the timing - *ORBIT_TIME* and *PP_TIME* words.

***ORBIT_TIME* word, write and read:**

Address: H"**170**"

Data bits	Content
D[11..0]	BC number that is the start of ORBIT *Inhibit* interval(0 - 3563)

Note: Control software *must* prevent attempts to write values higher than 3563.

The ORBIT *Inhibit* interval is 44 BCs long (*ScopeProbe* output A, code 22); it is followed by the broadcast frame transmission (ORBIT transmit, *ScopeProbe* output B, code 24); at the end of the transmissions (16 BCs), the TTCrx's internal *BC Counter* is reset.

***PP_TIME* word, write and read:**

Address: H"**171**"

Data bits	Content
D[11..0]	BC number that is the start of PP *Inhibit* interval (0 - 3563)

Note: Control software *must* prevent attempts to write values higher than 3563.

The PP *Inhibit* interval is 44 BCs long (*ScopeProbe* output A, code 23); it is followed by the broadcast frame transmission (PP transmit, *ScopeProbe* output B, code 25); at the end of the transmissions (16 BCs), the PP signal can be decoded at the TTCrx output.

Note: PP transmission shall be abandoned if its start (at the end of PP *Inhibit* interval - PP_TIME word) is due to occur during the ORBIT *Inhibit* interval (set by the ORBIT_TIME word).

N.2.3 TTC data transmission from the VME processor

The VME processor writes data into the TTC FIFO of the LTUvi board (*TTC_DATA* word); FIFO's capacity is 128 32-bit words; the *TTC_STATUS* word reads the FIFO's current status. The data transmission has the lowest priority (see the table in **N.2.1**); the transmission (42 serial bits; *Individually-addressed Frame* format - [3], Chapter 2) takes place during the *VME transmit* interval (*ScopeProbe* output B, code 28).

***TTC_DATA* word, write and read:**

Address: H"**172**"

Bit allocation:

Data bits	Content
D[31]	*Don't care*
D[30..17]	TTCrx address (14 bits; all 0: broadcast)
D[16]	E (1: external; 0: internal)
D[15..8]	Sub-address (8 bits)
D[7..0]	Data (8 bits)

The data format is identical to the TTCvi protocol - [4], *TTCvi Registers and VME Address Map*, *Long-format asynchronous cycles*; the two 16-bit words $C0 and $C2 are just transmitted as a single 32-bit word.

Note: The *TTC_DATA* read word returns the content of the last write access (*SpyMemory* option).

***TTC_STATUS* word, read only:**

Address: H"**72**"

Bit allocation:

Data bits	Content
D[0]	TTC FIFO empty
D[1]	TTC FIFO full

N.3 *ScopeProbe* signal selection - *LTUvi* board

The list of signals connected to the *ScopeProbe* outputs A and B is shown in the following tables; the list corresponds to the firmware version H"**B**X".The *ScopeProbe* option is described in [5], section 3.13; signal selection is controlled by the VME word *SCOPE_SELECT* [1].

Few words of explanation:

- Comment *selected* means: as received from the CTP in *Global* mode; or generated by the LTU emulator in *Stand-alone* mode.
- Comment *no errors/includes errors* explains whether the displayed signal is taken *before* or *after* the introduction of emulated errors.
- Comment *no delay/delay*, in case of the outputs *Channel A* and *Channel B*, explains whether the displayed signal is taken *before* or *after* the introduction of programmable ½BC delay.
- Comment *not registered* indicates that the displayed signal might show decoding glitches.
- Some signals - that are likely to be used as the scope trigger input - are available at both outputs A and B.

ScopeProbe output A

Code	*Firmware notation*	*Signal*	*Description*
0	bc	BC	40MHz LHC clock; includes delay; also at B0
1	ltu_select.orbit_sel	ORBIT	Selected ORBIT (1µs pulse); also at B17
2	ltu_select.prepulse_sel	PP request	PP request (25ns pulse); no errors
3	ltu_select.l1_strobe	L1 STROBE	Selected L1 STROBE; includes errors
4	ltu_select.l2_strobe	L2 STROBE	Selected L2 STROBE; includes errors
5	in_pulser	PULSER input	PULSER input signal
6	in_busy1	BUSY1 input	BUSY 1 input signal
7	in_busy2	BUSY2 input	BUSY 2 input signal
8	!write & strobe	VME read	VME read strobe
9	write & strobe	VME write	VME write strobe
10	strobe	VME strobe	VME strobe (read or write)
11	ttcvi.channel_b	Channel B	TTC Channel B output; no delay
12	minimax.busy_long	Long BUSY	*BusyProbe* BUSY_LONG output (25ns pulse); also at B30
13	adc_in	ADC input	Input to the ADC (LTU synchronisation)
14	ltu_select.err_request	Error request	Pending Error Request (*Error on Demand* option)
[15..16]	GND	GND	*Not used*; connected to ground
17	emu_st.start_all	START	Selected START signal (emulation trigger)
18	ltu_select.l0_sel	L0	Selected L0 (25ns pulse); no errors
19	vme_clock	VME clock	16MHz VME clock
20	ltu_select.l1	Channel A	TTC Channel A output no delay
21	ltu_select.l1_sel	L1 only	Selected L1 (25ns pulse); no errors
22	ttcvi.orbit_inhibit	ORBIT inhibit	ORBIT inhibit interval; 44 BCs; precedes ORBIT transmission (ORBIT select, B24)
23	ttcvi.pp_inhibit	PP inhibit	PREPULSE inhibit interval; 44 BCs; precedes PREPULSE transmission (PP select, B25)
24	ttcvi.vmefifo_write	VME TTC write	VME FIFO write strobe (25ns pulse)
25	ttcvi.ttc_busy	TTC BUSY	TTC Channel B transmission in progress
[26..31]	GND	GND	*Not used*; connected to ground

ScopeProbe output B

Code	*Firmware notation*	*Signal*	*Description*
0	bc	BC	40MHz LHC clock; includes delay; also at A0
1	in_bc	BC input	40MHz LHC clock; input signal, no delay
2	out_orbit	Channel B output	TTC Channel B output; includes delay and errors
3	out_prepulse	PP output	PP request (25ns pulse); includes errors (*The output is not used*)
4	out_l10	L0 output	L0 output; includes errors
5	out_l1	Channel A output	TTC Channel A output; includes delay and errors; L0 *and* L1 if L0 over TTC option
6	ltu_select.l1_data	L1 DATA	Selected serial L1 DATA; registered
7	ltu_select.l2_data	L2 DATA	Selected serial L2 DATA
8	emu_st.start	Emulation start	Start of the emulation sequence (not registered)
9	ltu_busy.busy	BUSY	LTU internal BUSY; all constituents
10	l1fifo_wr.l1fifo_empty	L1FIFO empty	*L1 Message* FIFO empty status
11	l2fifo_wr.l2fifo_empty	L2FIFO empty	*L2 Message* FIFO empty status
12	l1fifo_wr.l1nearly_full	L1FIFO full	*L1 Message* FIFO nearly full status
13	l2fifo_wr.l2nearly_full	L2FIFO full	*L2 Message* FIFO nearly full status
14	ltu_select.any_error	Any error	Any error signal (25ns pulse)
15	emu_lg.l1_strobe	Emu L1 STROBE	L1 STROBE signal from the emulator
16	emu_lg.l2_data	Emu L2 DATA	Serial L2 DATA from the emulator
17	ltu_select.orbit_sel	ORBIT	Selected ORBIT (1µs pulse); also at A1
18		L2a strobe	L2a strobe signal (25ns pulse)
19		L2r strobe	L2r strobe signal (25ns pulse)
20	bc_error	BC error	BC error flag
21	ltu_select.l1_only	L1 only	Selected L1 (25ns pulse); includes errors
22	ltu_select.l1_data_sel	L1 DATA (nr)	Selected serial L1 DATA; not registered
23	ttcvi.pp_request	PP pending	Pending PREPULSE request
24	ttcvi.orbit_select	ORBIT transmit	ORBIT transmission in progress (17 BCs)
25	ttcvi.pp_select	PP transmit	PP transmission in progress (17 BCs)
26	ttcvi.l1_select	L1 transmit	L1 word transmission in progress (43 BCs)
27	ttcvi.l2_select	L2 transmit	L2 word transmission in progress (43 BCs)
28	ttcvi.vme_select	VME transmit	VME TTC transmission in progress (43 BCs)
29	ttcvi.vmefifo_empty	VME FIFO empty	VME TTC FIFO empty status
30	minimax.busy_long	Long BUSY	*BusyProbe* BUSY_LONG output (25ns pulse); also at A12
31	GND	GND	Not used; connected to ground

N.4 Font panel LEDs - update for the *LTUvi* board

The logic and the operation of the LTU's front panel LEDs have been fully described in [1], section 3.3. In the *LTUv*i version of the board, the **Spare** LED has been attributed a somewhat different meaning:

Spare LED: *on* - if *Global Mode*; off - *if Stand-alone Mode*

Note: The LEDs **PP**, **L0** and **L1** do not display signals that are "masked" by the error-generating logic.

N.5 Font panel connections - update for the *LTUvi* board

Front panel input and output connections of the original LTU have been described in [5], section 3.5.6. The following updates apply to the *LTUvi* version of the board:

Spare: ECL output of the **BC** clock. The clock is a delayed **BC** input from the TTCex board; it is the main clock of the LTUvi's FPGA.

L1: *Channel A* connection to the TTCex board (ECL output); normally, the **L1** signal, but, in case of the "*L0 over TTC*" option, both the **L0** (code B"10") and the **L1** (code B"11") signals.

ORBIT: *Channel B* connection to the TTCex board (ECL output).

N.6 Cable connections in the TTC partition - *LTUvi* board

Cable connections in the original ALICE TTC partition are shown in [5], section 3.14.2, **Figure 3.14.1**; the figure has been reproduced here (**Figure A**) to ease the comparison. Connections in the new LTUvi partition are shown in **Figure B**.

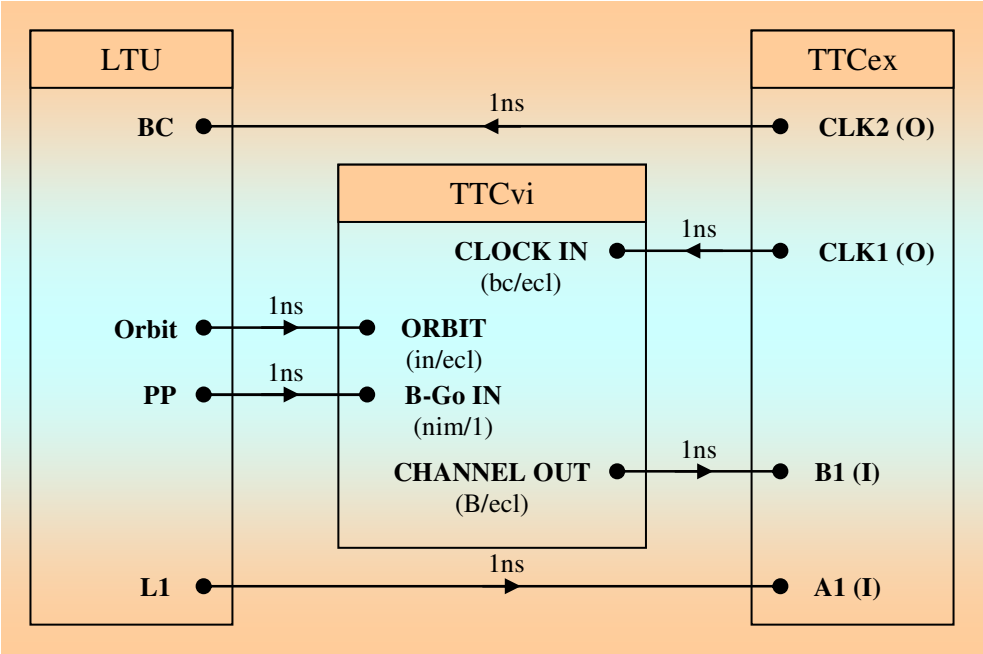

Figure A Connections in the TTC partition (LTU version - *old*)

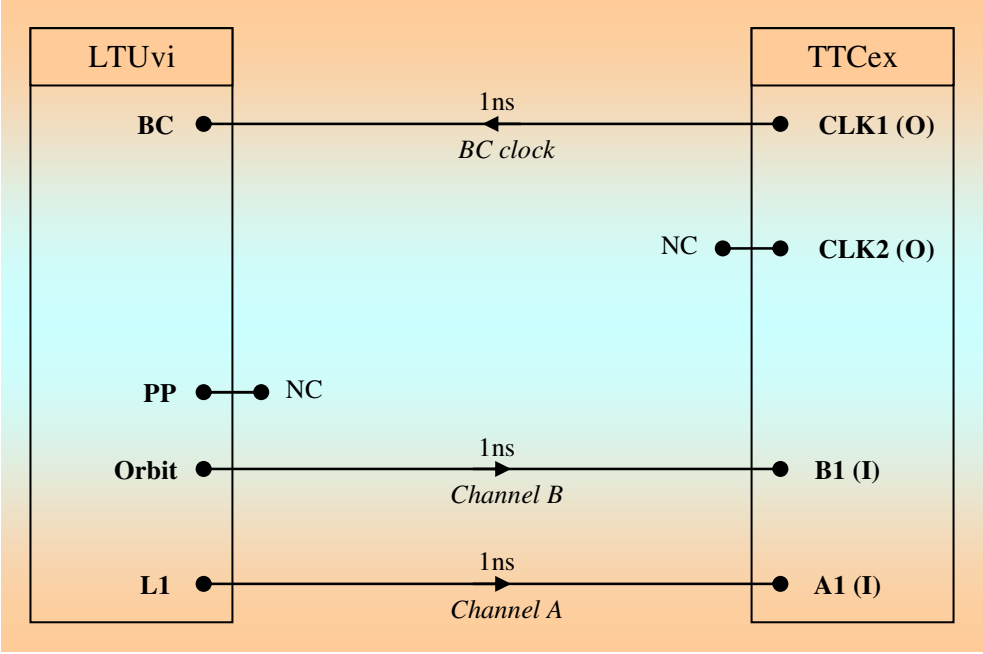

Figure B Connections in the TTC partition (***LTUvi*** version - *new*)