File: ltuvi_timing.doc
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Timing of the ALICE TTC partition - *LTUvi* version

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1 Introduction

This document provides the *mandatory rules* for setting the timing in sub-detector TTC partition of the ALICE trigger system; the details of timing requirements and the setting procedures are explained elsewhere ([1], section **3.14**). The note contains formulae, definitions, comments, a number of examples, *etc*.

In normal operation, the correct timing of the TTC partitions shall be set automatically by the trigger system control software. In *Stand-alone* mode, for testing purposes, sub-detectors might decide to make their own timing adjustments; even then, the requirements explained in [1] and the rules set in this document must be followed in order to avoid intermittent errors.

Current configuration of the ALICE TTC partition consists of the LTUvi board [1][2][3] and the TTCex opto-transmitter [4]; the connections within the partition are shown in [3], **Figure B**; a photograph in **Figure 1.1** depicts a typical layout. The original configuration - that used to include the TTCvi board - is now considered *obsolete* and it is *no longer supported*.

Figure 1.1 A typical layout of the ALICE TTC partition

2 General comments

2.1 Phase of the TTCrx BC clock

The phase of the **BC** clock at the output of the TTCrx chip (**Clock40**, **Clock40Des1**, **Clock40Des2**) is locked to the TTCex clock; the phase is *not affected* by the timing of either the CTP (BC_DELAY on the BUSY board) or the LTU (BC_DELAY_ADD).

2.2 Phase of the L0 in "*L0 over TTC*" option

In case of the "*L0 over TTC*" option [5], both time-critical signals **L0** and **L1** are transmitted over the TTC *Channel A*; the phase of both signal - at the output of the TTCrx chip, in respect to the local BC clock - is "stable": it is always phase-locked to the TTCex clock and *not affected* by the timing of either CTP or the LTU.

> Note: On the other hand, a change of the CTP timing could affect - and probably will - the *Event -to-L0* delay; just a reminder…

2.3 Phase of the L0 in "*L0 over cable*" option

In case of the "*L0 over cable*" option, the phase of the **L0** signal at sub-detector's front-end in respect to the local clock (*always* locked to the TTCex clock, see section **2.1**) depends on the CTP timing in *Global* mode and the LTU timing in *Stand-alone* mode.

A possibility to change the phase/to delay the CTP's **BC** clock is required in order to be able to "track" the last arriving **L0** input and, by doing so, to minimise the **L0** latency. Such changes are going to be infrequent, always announced in advance, with enough time left to sub-detectors to "tune" their electronics. Sub-detectors that use the "*L0 over cable*" option *must be able* to "re-tune" to the modified **L0** phase without physical access to their front-end electronics; the obvious options are the front-end reconfiguration, a change of programmable settings, *etc*.

2.4 Identical timing in both *Global* and *Stand-alone* modes - *harmonisation*

The LTU must ensure that the timing of trigger sequences as seen by sub-detector's front-end electronics in *Stand-alone* mode is *identical* to the timing used in the *Global* mode; in order to achieve that, the LTU's time-settings must always be *harmonised* with a current time-setting of the CTP. A term *harmonised* shall be often used in the following text; always with the same meaning: the LTU time setting that reproduces in *Stand-alone* mode the timing set by the CTP in Global mode.

The timing of trigger sequences in *Stand-alone* mode is defined by the setting of the L1_DELAY, L2_DELAY and the ORBIT_BC control words; their content, on the other hand, *has no effect* on the timing in *Global* mode.

The words BC_DELAY_ADD, TTC_INTERFACE, ORBIT_BC, ORBIT_TIME and PP_TIME affect the operation in both *Global* and *Stand-alone* modes; with a correct setting - a *harmonised* setting - they produce identical results in both modes.

3 Synchronisation of the LTU - setting of the BC_DELAY_ADD register

The LTU synchronisation procedure measures the phase (time of transition) of the signals generated by the CTP and clocked by the CTP's **BC** clock, in respect to the LTU's **BC** clock. The measurement provides the *Transition Time* ($\mathbf{T_{tr}}$) - the BC_DELAY_ADD content at which the delay plot obtains the minimum value. A typical plot is shown in **Figure 3.1**; the corresponding value of the $\mathbf{T_{tr}}$ is 24.

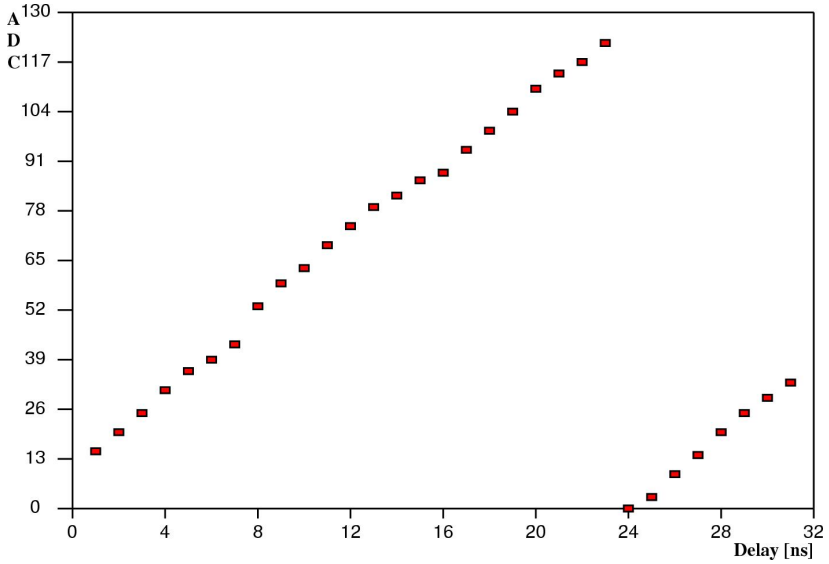

Figure 3.1 Typical plot of the LTU synchronization measurement; $\mathbf{T_{tr}}$ is 24

In *Global* mode, the CTP signals are sampled on the LTU board with a negative edge of the LTU's **BC** clock. The clock is generated on the TTCex board and delayed, on the LTU board, by a number of *ns* equal to the content of BC_DELAY_ADD register (0 to 31). When the register content is $\mathbf{T_{tr}}$, the negative edge of the clock samples the input signal at, approximately, the middle of the pulse, with a maximum and symmetric safety margin (~ ± ½BC).

In *Global* mode, the **L0** signal that appears at the LTU front panel output is not affected by any LTU setting - it is just the original CTP signal re-transmitted; its phase is set by the working content of the BC_DELAY register on the BUSY board. In order to achieve the same phase of the **L0** output in *Stand-alone* mode - when the signal is generated by the CTP emulator logic on the LTU board - the content of the BC_DELAY_ADD register must be set according to the following formula:

$$[\text{BC_DELAY_ADD}] = (\mathbf{T_{tr}} - 2)_{\text{modulo } 25} \qquad \textbf{[3.1]}$$

Examples: For $\mathbf{T_{tr}}$ = 17, [BC_DELAY_ADD] = 15; for $\mathbf{T_{tr}}$ = 1, [BC_DELAY_ADD] = 24; for $\mathbf{T_{tr}}$ = 0, [BC_DELAY_ADD] = 23; *etc.*

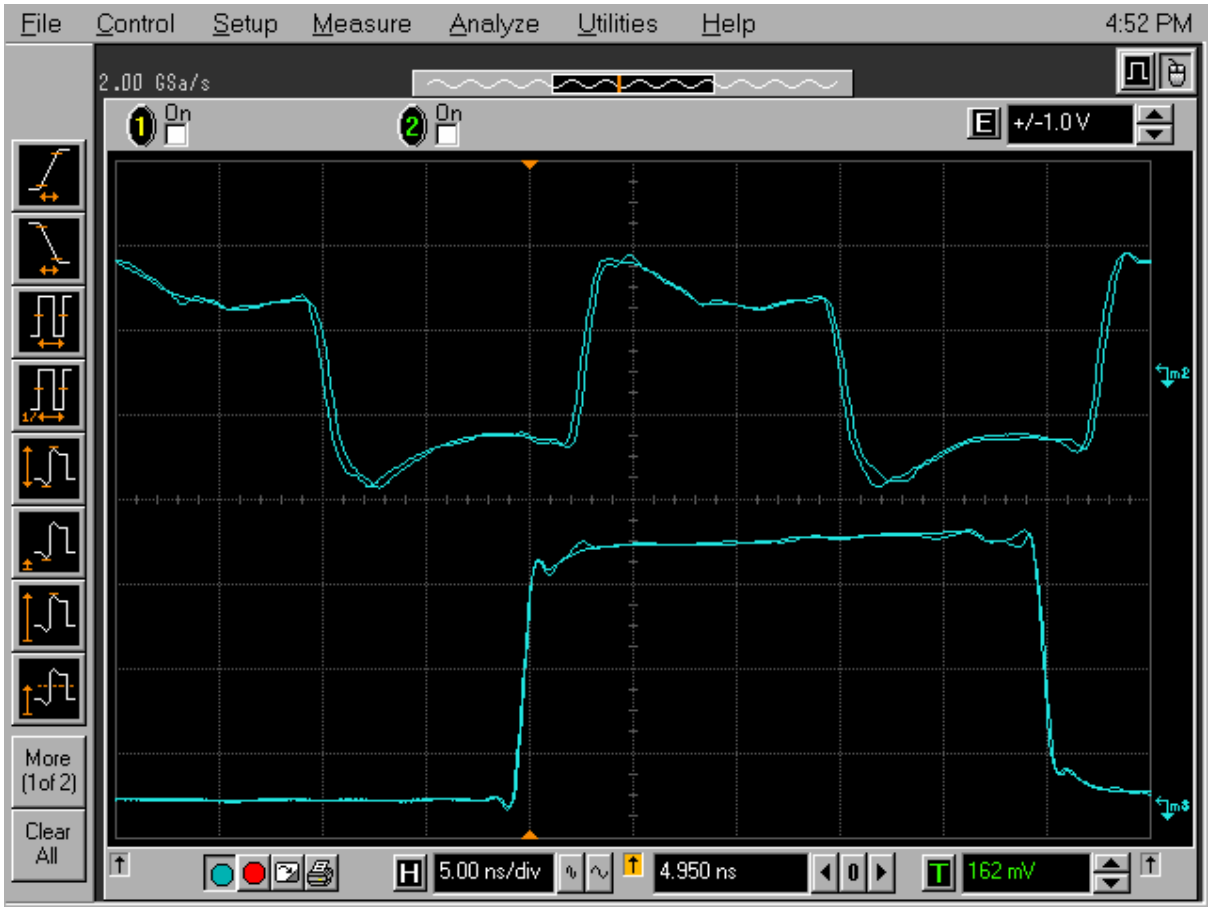

Figure 3.1 Identical phase of the **L0** output in *Global* and *Stand-alone* modes

Trace m1, m2: **CLK1(O)**, TTCex board (ECL, AC coupling; scope-probe connection)
Trace m3, m4: **L0** output**,** LTU board (*ScopeProbe* channel B, selection code 4)

Verification**:** **Figure 3.1** depicts the phase of the **L0** output (trace **m3** - *Global* mode; trace **m4** - *Stand-alone* mode) in respect to the TTCex clock (trace **m1** - *Global* mode; trace **m2** - *Stand-alone* mode), with the BC delay set using **Formula 3.1** - the phase shift is hardly noticeable. The signals have been generated using the test CTP in the Trigger Lab at CERN, in the TTC partition code-named "HMPID": the **L0** signal has been taken from the *ScopeProbe* channel B, selection code 4; the TTCex **BC** clock has been connected to the TTCex CLK1 output, using the "Y" adapter and a scope-probe, the synchronisation has given $\mathbf{T_{tr}} = 26$; the corresponding setting for the BC delay has been [BC_DELAY_ADD] = 24.

Very similar waveforms have been observed in the test "MUON" partition with $\mathbf{T_{tr}} = 26$ and for [BC_DELAY_ADD] = 24.

***Mandatory Rule 3.1*:**

For any change of the CTP timing (a change of the BC_DELAY content - BUSY board; a change of the BC input cable - BUSY board; a change of the CTP to LTU cable; etc.*), perform the LTU synchronisation, find a new value of the* $\boldsymbol{T_{tr}}$ *and then set the [BC_DELAY_ADD] according to* ***Formula 3.1****.*

4 Setting of the ORBIT_BC register

When the setting of ORBIT_BC register (on the LTU board) is *harmonised* with the BC_OFFSET setting (on the L0 board), the lead time of the **Prepulse** in respect to the calibration trigger **L0** (PP_TIME setting) and the *Mini ID* mismatch correction (ORBIT_TIME setting) *remain the same* in both *Global* and *Stand-alone* modes.

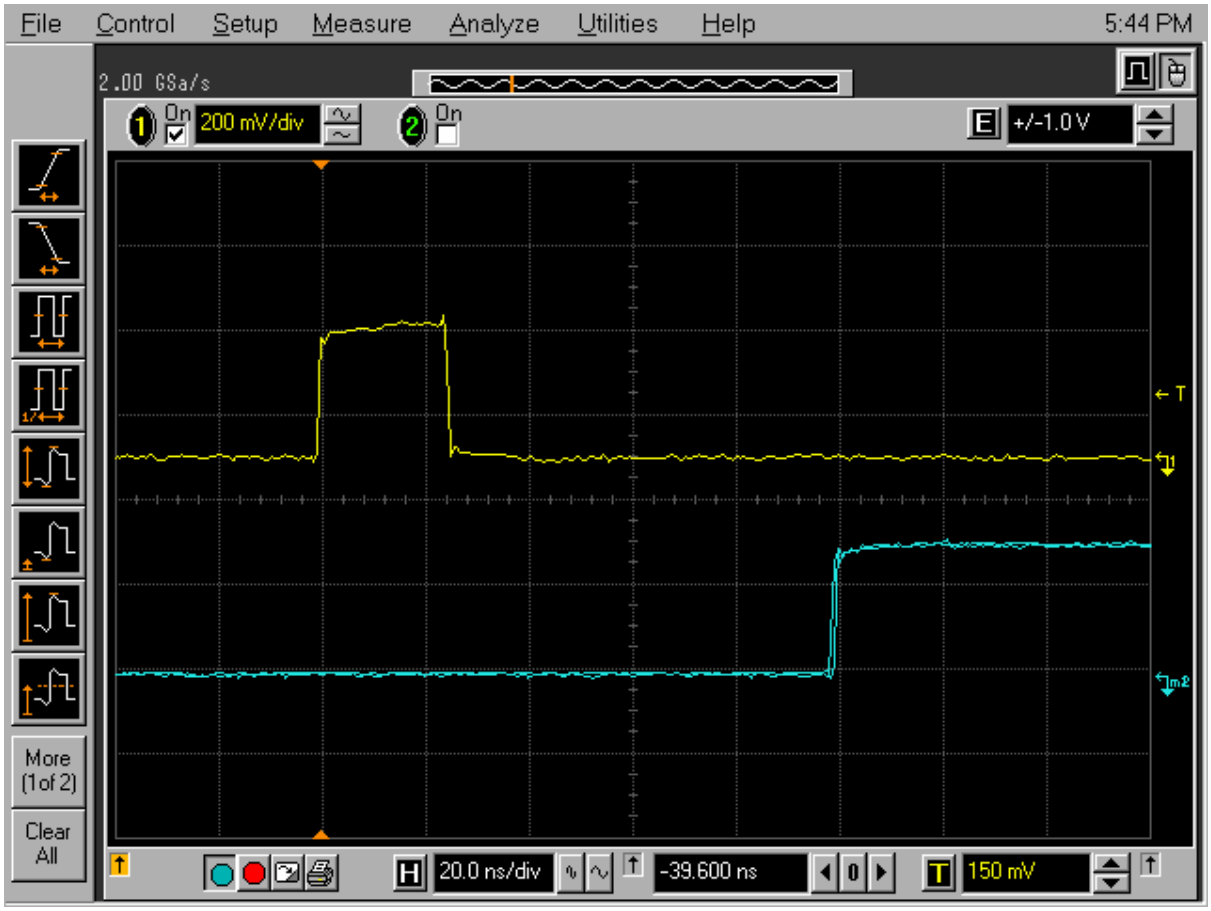

Figure 4.1 Identical timing of the **ORBIT** signal in respect to the calibration **L0** in *Global* and *Stand-alone* modes

Trace **1**: Calibration **L0** in *Global* and *Stand-alone* modes; LTUvi board, *ScopeProbe* - channel **B**, selection code 4

Trace **m1/m2**: Front edge of the **ORBIT** pulse (1µs wide) in *Global* and *Stand-alone* modes; LTUvi board, *ScopeProbe* - channel **A**, selection code 1

***Mandatory Rule 4.1*:**

The setting of ORBIT_BC register on the LTU board must always "track" the setting of BC_OFFSET register on the L0 board:

$$[\text{ORBIT_BC}] = ([\text{BC_OFFSET}] - 4)_{\text{modulo } 3564} \qquad \textbf{[4.1]}$$

Example: Since the new *TTC Machine Interface* (TTCmi) can provide a programmable delay of the **ORBIT** input to the BUSY board, it is likely that the BC_OFFSET on the L0 board shall always be **0**; the corresponding setting of the ORBIT_BC, according to **Formula 4.1**, is **3560**. With those settings, the delay between the calibration **L0** (always in the bunch crossing 3556: [CALIBRATION_BC] = 3556 - LTU board; [TC_SET D[11..0]] = 3556 - L0 board) and the front edge of the **ORBIT** pulse (1µs wide) is the same in both *Global* and *Stand-alone* modes. This is shown in **Figure 4.1**.

5 Setting of the Prepulse lead time T_{ppl0} - PP_TIME register

Definition: The **Prepulse** signal is transmitted *via* the TTC *Channel B* as a broadcast command with the priority set to 1 (there are 5 priority levels, 0 to 4; 0 is the highest priority - see [3], section **N.2.1**); all the six user-bits D[7..2] are asserted (the bits are cleared in *all* other applications). At the output of TTCrx chip, the **Prepalse** is decoded as a coincidence of the *Broadcast Strobe* (**BrcstStr1** or **BrcstStr2**) and any of the asserted user-bits D[7..2].

It is appropriate, therefore, to define the **Prepulse**-to-Calibration **L0** time ($\mathbf{T_{ppl0}}$) as the time between the corresponding *Broadcast Strobe* (**BrcstStr1** or **BrcstStr2**) and the calibration **L0** at the TTCrx output **L1Accept** - the "*L0 over TTC*" option. Providing that all the TTCrx coarse and fine delays are set to 0 and that the decoding of **Prepulse** and **L0** adds symmetrical delays in both channels, the following **Formula 5.1** gives an *exact* $\mathbf{T_{ppl0}}$ value for the "*L0 over TTC*" option; for any deviation from those default conditions; the result has to be appropriately corrected. A more serious deviation is likely in case of the "*L0 over cable*" option; even then the correction could be calculated - at least approximately (for details see section **8**), but the proper value is best found experimentally.

With *harmonised* settings of ORBIT_BC and BC_OFFSET (section **4**), the setting of the PP_TIME for a desired lead time $\mathbf{T_{ppl0}}$ (expressed in BCs) of the **Prepulse** in respect to the calibration trigger **L0** is defined by the following formula:

$$[\text{PP_TIME}] = [\text{CALIBRATION_BC}] - 66 - \mathbf{T_{ppl0}} \qquad \textbf{[5.1]}$$

Since the CALIBRATION_BC is always 3556, the formula can be simplified:

$$[\text{PP_TIME}] = 3490 - \mathbf{T_{ppl0}} \qquad \textbf{[5.2]}$$

The set timing is equally valid in both *Global* and *Stand-alone* modes.

Example: For a desired $\mathbf{T_{ppl0}}$ of 80 BCs (~ 2µs), the corresponding setting is $[\text{PP_TIME}]_{2\mu s} = 3410$

Verification: **Figure 5.1** shows the TTCrx outputs involved in decoding of **Prepulse**, and their timing for two different settings of the PP_TIME register; the signals have been generated on the TTCrx test board.

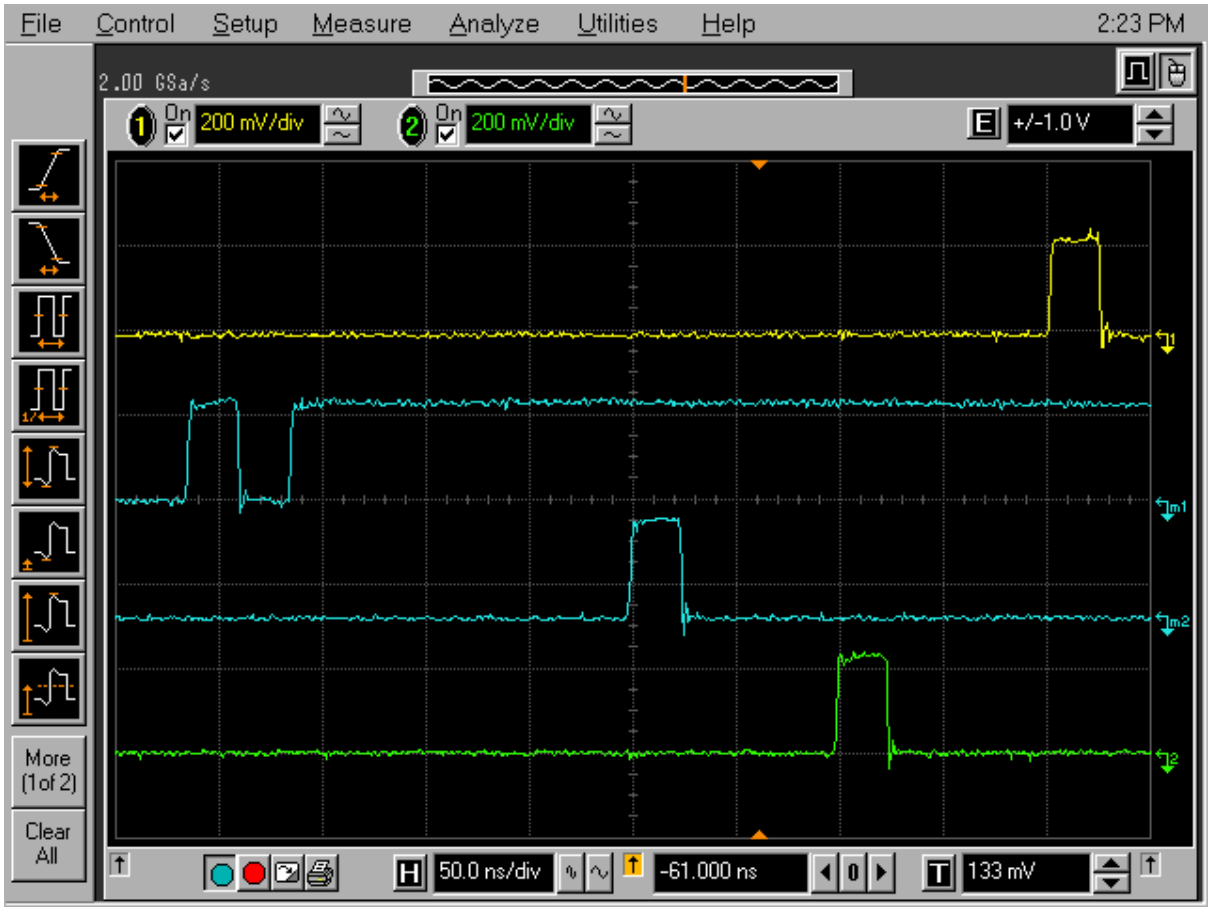

Figure 5.1 **Prepulse** to **L0** delay at the TTCrx output for two different settings of the PP_TIME register: 3482 and 3486

Trace **1**: Calibration **L0** signal - TTCrx output **L1Accept** ("*L0 over TTC*" option).

Trace **m1**: Last few serial bits of the **Prepulse** broadcast command - TTCrx output **Serial_B_Channel**; [PP_TIME] = **3482**.

Trace **m2**: Data strobe of the **Prepulse** broadcast command - TTCrx **BrcstStr1** output; [PP_TIME] = **3482**; the $\mathbf{T_{pplo}}$ time is **8** BCs (200ns) - in full agreement with **Formula 5.1/5.2**.

Trace **2**: Data strobe of the **Prepulse** broadcast command - TTCrx **BrcstStr1** output; [PP_TIME] is increased to **3486**; the corresponding $\mathbf{T_{pplo}}$ time is **4** BCs (100ns).

Verification: **Figure 5.2** depicts the measurement of the $\mathbf{T_{pplo}}$ for $[PP_TIME]_{2\mu s}$ = 3410; the delay of 1.9995 µs is indeed exactly 80 periods of the 40.079 MHz BC clock.

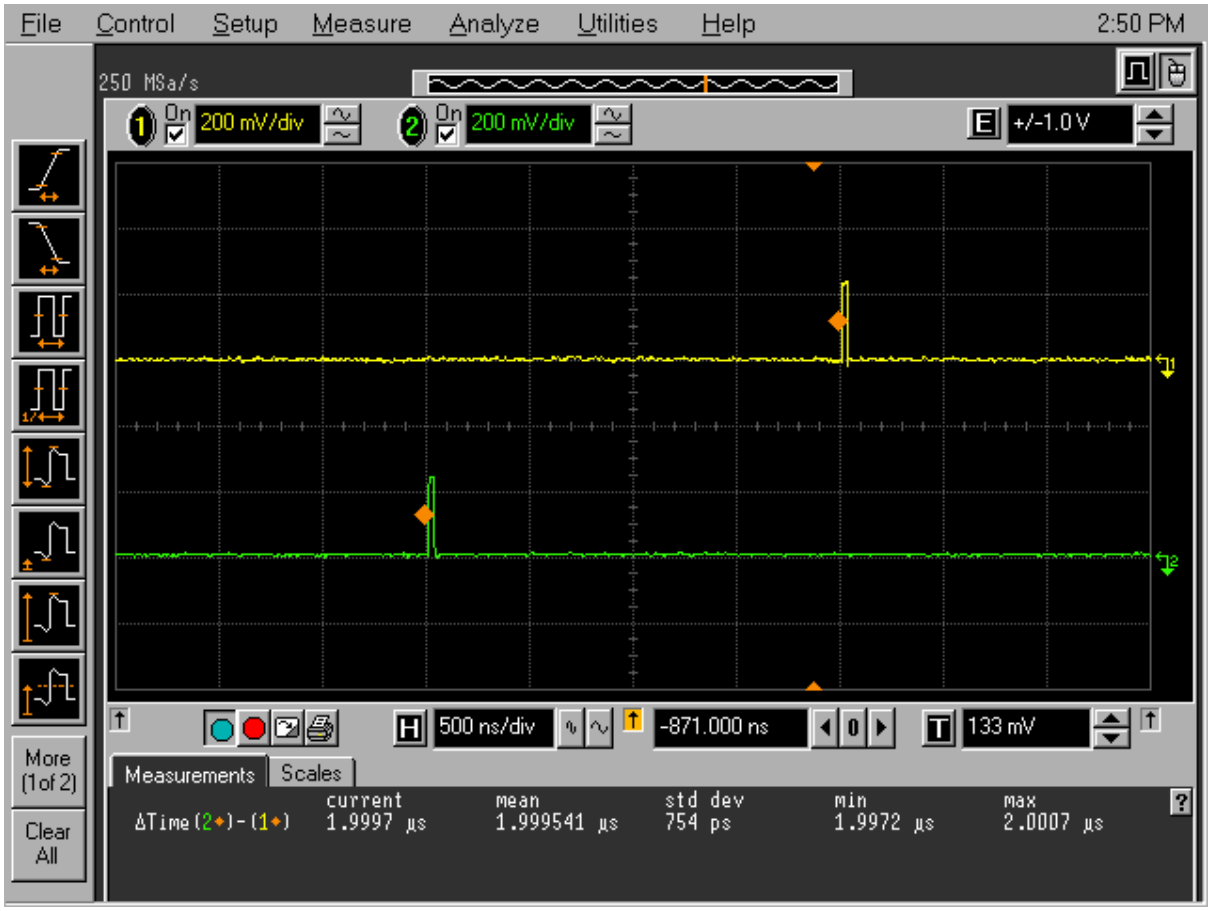

Figure 5.2 **Prepulse** to **L0** delay of 2µs measured at the TTCrx output; [PP_TIME]=3410

Trace 1: Calibration **L0** signal - TTCrx output **L1Accept** ("*L0 over TTC*" option).
Trace 2: Data strobe of the **Prepulse** broadcast command - TTCrx **BrcstStr1** output; [PP_TIME] = **3410**.

6 *Correction of the Mini ID mismatch - ORBIT_TIME register*

In the trigger/DAQ jargon, the *Mini ID* is the event bunch crossing number read from the TTCrx BC counter at the time of arrival of the **L1** trigger signal. The value should be identical to the event BC number contained in the *L2a Message*, but the DAQ tolerates the difference as long as it remains the same throughout the run. The difference - the *mismatch* - can be reduced to zero by adjusting the content of the ORBIT_TIME register (LTU board).

The *correction* tracks the setting of *L1 time* (DELAY_L0 on the L1 board; L1_DELAY on the LTU board); normally, its value is close to the current setting of the L0-to-L1 time (in BCs); the exact value - the setting that brings the *mismatch* to zero - needs to be found experimentally. The correction holds in both *Global* and *Stand-alone* modes.

Apart from the *mismatch* correction, the content of the ORBIT_TIME *does not* affect any other time setting - the *mismatch* correction is its *only* application.

7 TTCex interface - BC_DELAY_ADD and TTC_INTERFACE registers

The *set-up time* ($\mathbf{t_{su}}$) and the *hold time* ($\mathbf{t_h}$) requirements for the *Channel A* and *Channel B* signals are "mapped" to the **A** and **B** inputs of the TTCex board; they are defined in respect to the negative and the positive edge, respectfully, of the clock output **CLK**. The following values are quoted in the board's documentation [4]:

$$\mathbf{t_{su}} = 5.1\text{ns}$$
$$\mathbf{t_h} = 3.4\text{ns}$$

The values appear excessive since the board employs high-speed circuits. A closer inspection of the board schematics, taking into account the ICs' timing specs, reveals that the given values include - and justifiably so - a "healthy" safety margin of approximately 4ns; the details of the time analysis are presented in **Figure 7.1**.

The phase of the *Chanel A/Channel B* inputs depends upon the wiring of the TTC partition (cable length) and the content of the BC_DELAY_ADD register. The wiring in the ALICE experimental cavern is identical for all sub-detectors - see [3], **Figure B**; the scheme is also used for the test systems in the Trigger Lab; the wiring of test setups in collaboration home institutes should be done in the same way. The phase measurement performed on any of those systems should produce identical results and the conclusions are applicable to all.

Measurements of the phase of the input **A/B** in respect to the **CLK** output as a function of the BC_DELAY_ADD setting have been done on two test setups in the trigger lab, code-named "HMPID" and "MUON"; the measurements have been repeated on two systems in order to verify the consistency; the results are presented in **Table 7.1**. The phase difference has been measured using scope-probes connected directly to the TTCex inputs/outputs *via* a LEMO "Y" adapter; a typical scope display is shown in **Figure 7.2**. Positive values in **Table 7.1** refer to the phase/time to the *next* corresponding (positive or negative) clock edge - a check of potential *set-up time* violation; negative values are the phase in respect to the *preceding* clock edge - a check of potential *hold time* violation. The measurements have been done only for settings around the time violation area (5.1ns/-3.4ns), in the *no delay* and the *delay* modes (the delay of ½BC option for *Channel A/Channel B* input is controlled by data bits D[0..1] of the TTC_INTERFACE word - [3], section **M.2**).

Part of the TTCex board schematics.

The *propagation delay* and the *set-up* and *hold* times are taken from the IC data sheets at the 25ºC temperature.

40C and **40C*** signals are the 40.079 MHz clock and its complement.

Calculation of the MC10E131 *set-up time* as "seen" from the TTCex inputs **A/B** and the clock output **CLK** - *the worst case*.

Calculation of the MC10E131 *hold time* as "seen" from the TTCex inputs **A/B** and the clock output **CLK** - *the worst case*.

MC10E131 *set-up* and *hold* times "mapped" to the TTCex inputs **A/B** and the clock output **CLK**.

The declared TTCex *set-up* and *hold* times appear to contain a "healthy" safety margin of ~4ns.

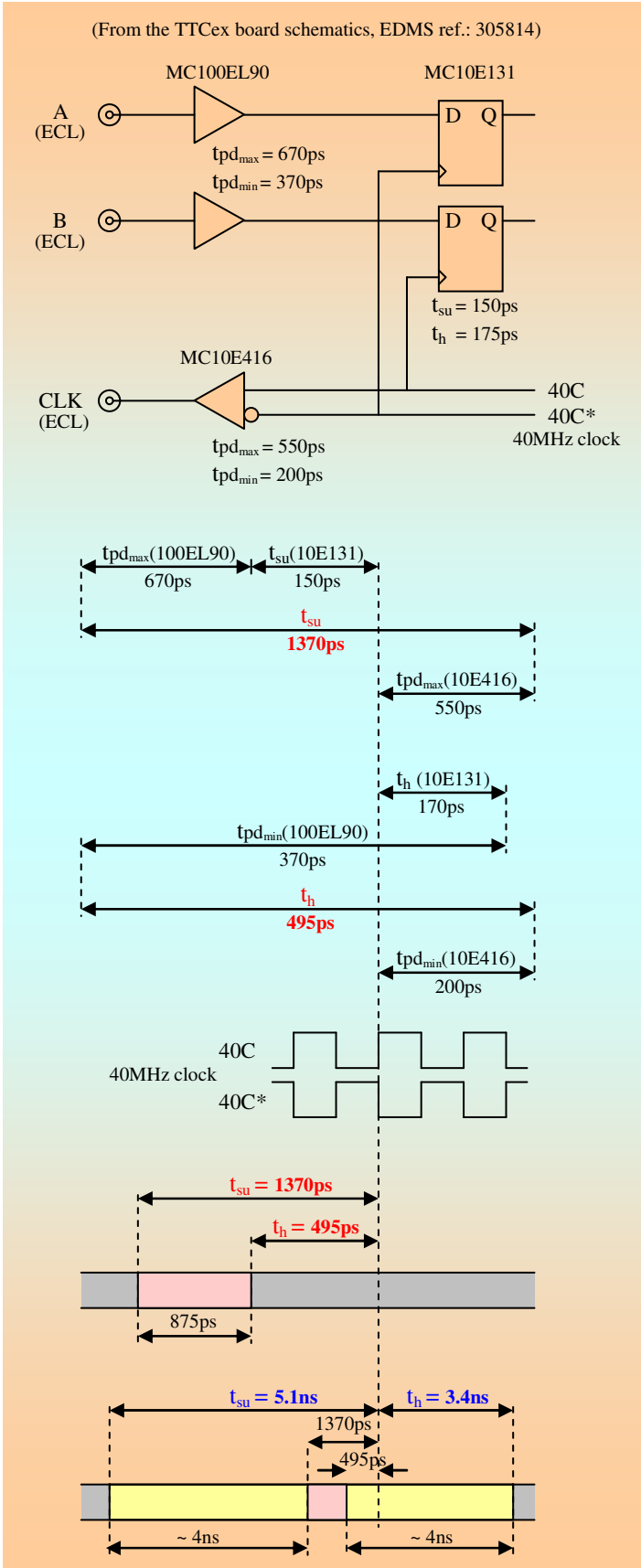

Figure 7.1 Evaluation of the *set-up time* ($\mathbf{t_{su}}$) and the *hold time* ($\mathbf{t_h}$) requirements for *Channel A* and *Channel B* inputs of the TTCex board.

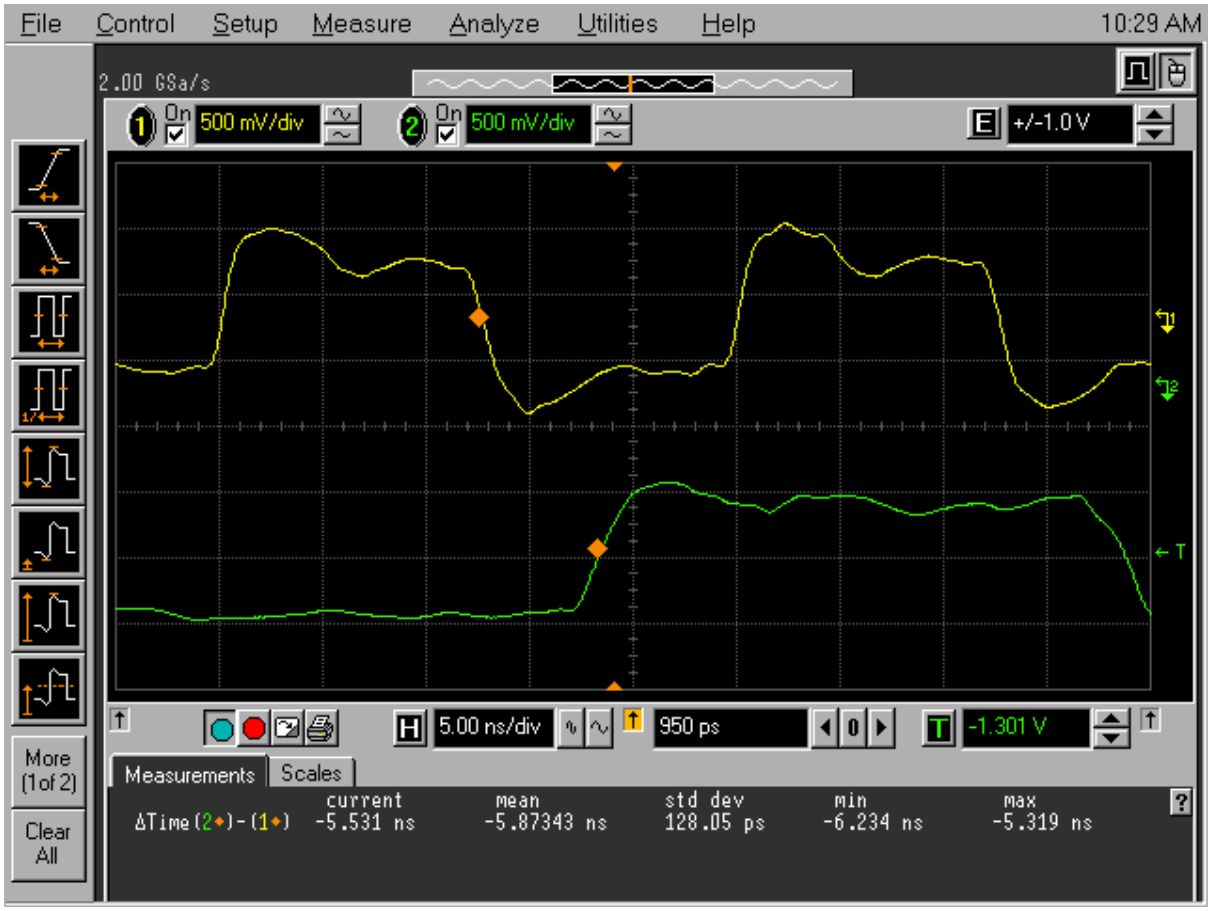

Figure 7.2 Typical measurement of phase of the TTCex input

[BC_DELAY_ADD] = 17; [TTC_INTRFACE] = 0
Trace 1: BC clock, TTCex output CLK1
Trace 2: *Channel A* input of the TTCex board

The measurements shown in **Table 7.1** justify the selection of the *delay*/no *delay* option (TTC_INERFACE word) for the *Channel A* (data bit D[0]) and the *Channel B* (data bit D[1]) signals as a function of the BC_DELAY_ADD content; the appropriate settings are shown in the right-most column; for software applications, the cleaned-up version is reproduced as **Table 7.2.**

***Mandatory Rule 7.1*:**

Following the LTU synchronisation *procedure, define* - ***Formula 3.1*** *- the setting of BC_DELAY_ADD word (0 to 31, but values higher than 25/26 should never be required); set the data bits D[1..0] of TTC_INTERFACE word according to* ***Table 7.2****; assert the data bit D[3] if the sub-detector uses the"L0 over TTC" option (bit D[2] is not used* - don't care *state).*

Results of a recent synchronisation (Anton Jusko, 22.07.2008) of all ALICE TTC partitions are shown in **Table 7.3** - *BC delay (measured*), together with the corresponding contents of the BC_DELAY_ADD word - *BC delay (setting*) - and the TTC_INTERFACE word. Those setting are currently used by the ALICE trigger system configuration software.

Table 7.1 Phase measurements of the *Channel A* and *Channel B* inputs (TTCex board) in the ALICE TTC partition

BC Delay	*Channel A*				*Channel B*				*TTC Interface*
	No delay D[0]=0		*Delay* D[0]=1		*No delay* D[1]=0		*Delay* D[1]=1		
D[4..0]	"HMPID"	"MUON"	"HMPID"	"MUON"	"HMPID"	"MUON"	"HMPID"	"MUON"	D[1..0]
0			1.79ns	1.39ns	1.89ns	1.85ns			10
1			0.33ns	-0.02ns	0.59ns	0.34ns			10
2									10
3									10
4			-2.43ns	-2.96ns	-2.51ns	-2.73ns			10
5	7.92ns	7.28ns	-3.40ns	-4.09ns	-3.33ns	-3.36ns			10
6	7.38ns	6.65ns	-4.01ns	-4.79ns	-3.84ns	-3.95ns	8.99ns	8.51ns	10
7	6.10ns	5.81ns	-5.35ns	-5.64ns	-4.99ns	-4.95ns	7.74ns	7.63ns	11
8	4.90ns	4.80ns	-6.47ns	-6.46ns	-6.13ns	-5.72ns	6.45ns	6.89ns	01
9	3.42ns	3.15ns					5.17ns	5.61ns	01
10							4.50ns	4.61ns	01
11							3.45ns	3.65ns	01
12									01
13									01
14									01
15	-1.79ns	-1.71ns							01
16	-2.49ns	-2.73ns							01
17	-3.85ns	-4.32ns					-2.12ns	-2.19ns	01
18	-4.73ns	-5.30ns	8.93ns	8.47ns			-2.89ns	-2.93ns	01
19	-6.01ns	-6.56ns	7.91ns	7.61ns	7.98ns	7.65ns	-4.02ns	-3.78ns	00
20			7.00ns	6.59ns	6.84ns	6.66ns	-4.87ns	-4.94ns	10
21			6.21ns	5.69ns	5.99ns	5.93ns	-5.73ns	-5.76ns	10
22			5.58ns	5.04ns	5.52ns	5.40ns			10
23			4.26ns	3.94ns	4.49ns	4.50ns			10
24			3.56ns	3.15ns	3.89ns	3.85ns			10
25									10
26									10
27									10
28									10
29									10
30	9.15ns								10
31	8.10ns						10.04ns	9.99ns	10

Table 7.2 Setting of the TTC_INTERFACE register as a function of the selected content of the BC_DELAY_ADD word

BC Delay	*TTC Interface*
D[4..0]	D[1..0]
0	10
1	10
2	10
3	10
4	10
5	10
6	10
7	11
8	01
9	01
10	01
11	01
12	01
13	01
14	01
15	01
16	01
17	01
18	01
19	00
20	10
21	10
22	10
23	10
24	10
25	10
26	10
27	10
28	10
29	10
30	10
31	10

Table 7.3 Current setting of the BC_DELAY_ADD and the TTC_INTERFACE registers in ALICE TTC partitions

Mnemonic	*BC delay (measured)*	*BC delay (setting)*	*L0 over TTC*	*TTC interface* D[3..0]
SDD	1	**24**	+	**1x10 A**
MCH	1	**24**		**0x10 2**
MTR	4	**2**		**0x10 2**
DAQ	3	**1**	+	**1x10 A**
SPD	4	**2**	+	**1x10 A**
TOF	6	**4**	+	**1x10 A**
V0	4	**2**	+	**1x10 A**
TRD	8	**6**	+	**1x10 A**
ZDC	7	**5**		**0x10 2**
EMC	10	**8**	+	**1x01 9**
TPC	11	**9**	+	**1x01 9**
PMD	12	**10**		**0x01 1**
ACORDE	10	**8**	+	**1x01 9**
SSD	8	**6**		**0x10 2**
FMD	8	**6**	+	**1x10 A**
T0	7	**5**	+	**1x10 A**
HMPID	12	**10**		**0x01 1**
PHOS	12	**10**	+	**1x01 9**
CPV	10	**8**		**0x01 1**

8 Definition of the L1 time (T_{L1}) - setting of the L1_DELAY register

Although a *general* meaning of the *L1 time* is well understood, a check/a verification of it in different applications is likely to produce inconsistent claims since the measurement procedure is not clearly defined; the ambiguity could cause misunderstandings. The following definition is an attempt to provide a uniform approach: for a given setting, the correct value of the $\mathbf{T_{L1}}$ is a time/a delay between the **L0** and the **L1** pulses at the **L1Accept** output of the TTCrx chip. The same delay can be measured at the *Channel A* output of the LTU board - front panel connector **L1**; or, more conveniently, at the *ScopeProbe* outputs **A** (selection code 20) or **B** (code 5). A typical scope display is shown in **Figure 8.1.**

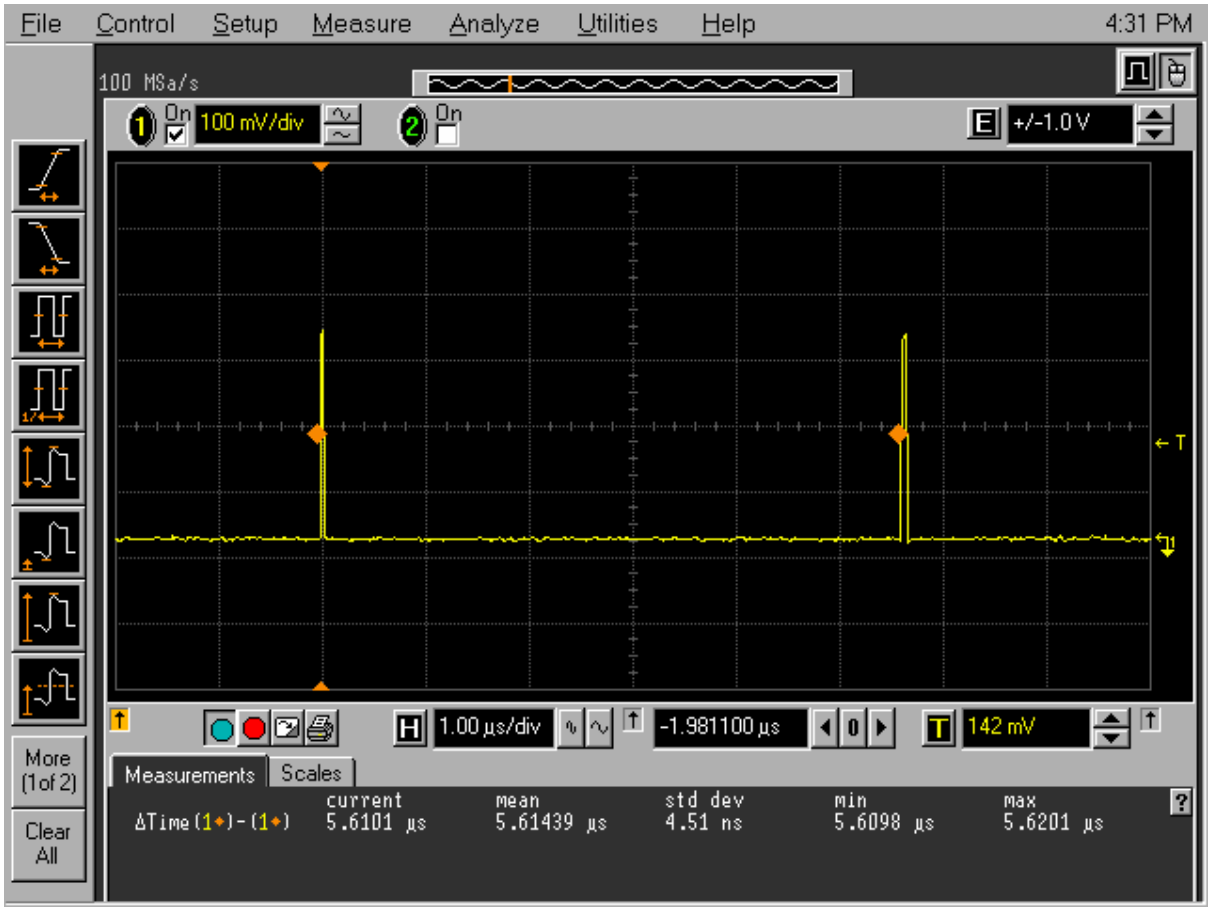

Figure 8.1 Measurement of the **L0** to **L1** delay ($\mathbf{T_{L1}}$) - "*L0 over TTC*" option

[L1_DELAY] = 244 (LTU board, *Stand-alone* mode)
[DELAY_L0] = 170 (L1 board, *Global* mode)
Trace 1: *Channel A* (*ScopeProbe* output B, selection code 5)

The following formulae give the setting of the L1_DELAY (LTU board, *Stand-alone* mode) and the DELAY_L0 registers (L1 board, *Global* mode) for a desired value of $\mathbf{T_{L1}}$ (in BCs):

$$[\text{DELAY_L0}] = \mathbf{T_{L1}} - 55 \qquad \textbf{[8.1]}$$

$$[\text{L1_DELAY}] = \mathbf{T_{L1}} - 1 \qquad \textbf{[8.2]}$$

or, to *harmonise* the settings:

$$[\text{L1_DELAY}] = [\text{DELAY_L0}] + 54 \qquad \textbf{[8.3]}$$

***Mandatory Rule 8.1*:**

In order to have identical timing in Global *and* Stand-alone *modes, the setting of the L1_DELAY (LTU board) and the DELAY_L0 (L1 board) registers should always be harmonised - set for the same value of* $\mathbf{T_{L1}}$.

Example: The *harmonisation* at work is demonstrated in **Figure 8.1**: with [L1_DELAY] = 224 and [DELAY_L0] = 170, the value of $\mathbf{T_{L1}}$ = 225 BCs (5.614μs) is measured in both *Global* and *Stand-alone* modes.

A general $\mathbf{T_{L1}}$ definition is only possible for the "*L0 over TTC*" option; in the "*L0 over cable*" case, the **L0** and the **L1** signals are transmitted over different media: over the cable (4.5ns/m propagation delay for the standard ALICE LVDS cable) and over the TTC optical link (4.9ns/m propagation delay of the single mode 1310nm fibre and ~ 100ns delay for the TTCex set-up time margin, the TTCex encoding and the TTCrx decoding logic - **Figure 8.2**). The "individual correction" for the "*L0 over cable*" option is dependent upon the layout - the length of the cable, the length of the fibre, *etc*. ; for a given layout, the correction is constant, it could be estimated by a calculation, but the only place it can be verified is sub-detector's front-end.

Figure 8.2 Measurement of the **L0/L1** propagation delay over the TTC optical link

[BC_DELAY] = 4 - ~9ns set-up time to negative clock edge
TTC_NTERFACE D[0] = 0 - no *Channel A* delay
Trace 1: **L0** output at the *L0* connector of LTU board
Trace 2: **L0** signal at the *L1Accept* pin of TTCrx chip

Figure 8.2 shows the measurement of skew between the **L0** signal at the *L0* output of the LTU board and the corresponding **L0** at the *L1Accept* pin of the TTCrx chip. The waveforms have been sampled with identical scope-probes; the length of the optical-fibre between the TTCex board and the TTCrx chip is 5m (24.5ns); the setting of [BC_DELAY] is 4, without *Channel A* delay (TTC_NTERFACE D[0] = 0), gives

~9ns of set-up time in respect to the next negative edge of the TTCex clock (**Table 7.1**) - which is close to a practical minimum. After the subtraction of the optical-fibre delay (5m, 24.5ns), the remaining **106ns** represent the "overhead" introduced by the *Channel A* signal encoding on the TTCex board and the signal decoding performed by the TTCrx logic. Identical delay is encountered by the **L1** signal.

9 Definition of the L1-to-L2 time (T_{L1L2}) - setting of the L2_DELAY register

Seen from sub-detector's side, the timing of the L2 trigger is not very precise: both the *L2a Message* and the *L2r Word* are transmitted *via* the TTC's *Channel B*; both are subject to queuing, delays, priority arbitration *etc*. In order to make the setting measurable and its verification possible, the definition of the L2 time has to be "moved" to the LTU's internal logic, ahead of the uncertainty of the *Channel B* transmission delay. The following definition offers a convenient compromise.

> The *L1-to-L2 time* $\mathbf{T_{L1L2}}$ is the delay between the **L1 Strobe** and the **L2 Strobe** signals inside the *LTU Logic* FPGA.

Both signals can be conveniently observed at the LTU's *ScopeProbe* outputs:

- **L1 Strobe**, output **A**, selection code 3
- **L2a Strobe**, output **B**, code 4 (coincides in time with more general **L2 Strobe**, output **A**, code 4)

In *Global* mode, the $\mathbf{T_{L1L2}}$ time is set by the CTP word DELAY_L1 (L2 board); in *Stand-alone* mode, on the other hand, the L2_DELAY word (LTU board) sets the *L0-to-L2 time* ($\mathbf{T_{L2}}$), while the *L0-to-L1 time* ($\mathbf{T_{L1}}$), is set separately by the L1_DELAY word.The difference makes the *harmonisation* formula somewhat more complicated:

$$[\text{DELAY_L0}] = \mathbf{T_{L1}} - 55 \qquad \textbf{[8.1]}$$

$$[\text{DELAY_L1}] = \mathbf{T_{L1L2}} - 64 \qquad \textbf{[9.1]}$$

$$[\text{L2_DELAY}] = \mathbf{T_{L1}} + \mathbf{T_{L1L2}} = \mathbf{T_{L2}} \qquad \textbf{[9.2]}$$

or, in order to *harmonise*:

$$[\text{L2_DELAY}] = [\text{DELAY_L0}] + [\text{DELAY_L1}] + 119 \qquad \textbf{[9.3]}$$

Providing that the L1_DELAY setting has already been harmonised (**Formula 8.2** or **8.3**), **Formula 9.3** assures in *Stand-alone* mode a value for $\mathbf{T_{L1L2}}$ identical to the one in *Global* mode.

Example: For $\mathbf{T_{L1}}$ = 225 BCs and $\mathbf{T_{L1L2}}$ = 3735 BCs, the corresponding settings for timing in *Global* mode would be:

[DELAY_L0] = $\mathbf{T_{L1}}$ - 55 = 170;
[DELAY_L1] = $\mathbf{T_{L1L2}}$ - 64 = 3671.

The harmonised settings in *Stand-alone* mode would be:

[L1_DELAY] = [DELAY_L0] + 54 = 224;
[L2_DELAY] = [DELAY_L0] + [DELAY_L1] + 119 = 3960.

Note: In the unlikely case that the full range of DELAY_L0 (9 bits) and of DELAY_L1 (12 bits) were used in *Global* mode, the range of the L2_DELAY (12 BITS) is not enough to enable harmonised emulation in *Stand-alone* mode. Just a comment…

10 Current setting of essential LTU timing-control words

The settings of *all* LTU words listed in **Table 10.1** are *essential* - otherwise the timing in TTC partition is likely to become unpredictable and certainly different from expected; the given formulae could produce wrong results.

Table 10.1 Current setting of essential LTU timing-control words

Control word	*Section*	*Setting*	*Comment*
L1_DELAY	**8**	**224**	**L0** to **L1** time: 225 BCs
L2_DELAY	**9**	**3960**	**L0** to **L2** time: 3960 BCs
BC_DELAY_ADD	**3,7**	*Sub-detector specific*	Use **Table 7.3**
TTC_INTERFACE	**7**	*Sub-detector specific*	Use **Table 7.3**
ORBIT_TIME	**6**	*Sub-detector specific*	Correct CDH mismatch
PP_TIME	**5**	*Sub-detector specific*	Use **Formula 5.1** or **5.2**
LAST_BC		**3563**	*System parameter*
PREPULSE_BC		**128**	*System parameter*
CALIBRATION_BC		**3556**	*System parameter*
GAP_BC		**3446**	*System parameter*
ORBIT_BC		**3560**	*System parameter*

The settings should also be used in test systems in home institutes in order to correctly emulate the application timing; this is particularly relevant for sub-detectors with "*L0 over cable*" option.

References

[1] *LTU - Preliminary Design Review*, Revision 1.0 [6]
[2] *LTU - Software Model*, Revision 0.1 [6]
[3] *LTUvi - Software Model Update* [6]
[4] *TTC Laser Transmitter (TTCex, TTCtx, TTCmx) User Manual,* TTC web site: http://ttc.web.cern.ch/ttc/
[5] *Proposal to Transmit L0 signal over TTC optical Link* [6]
[6] ALICE Trigger web site: ALICE-Projects-Trigger, or directly: http://epweb2.ph.bham.ac.uk/user/pedja/alice/