System timing

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Introduction

The adoption of the timing scheme for the ALICE system implies a compromise on three essential issues:

- the "quality" of the **BC** clock, distributed to the sub-systems;
- the ease, or otherwise, of the synchronisation of the experiment;
- the latency of trigger signals **L0** and **L1**.

The interface requirements of the TTC system must also be taken into consideration, especially those concerning the connections to the TTCvi and the TTCex boards, both part of the sub-detector TTC partition.

In preparation, a survey has been conducted of the timing requirements of the sub-detectors (see ***Timing issues - a questionnaire***, 10 July 2002). Also, an extensive exchange of messages with the TTC experts (Bruce Tailor, Per Gunnar Gällnö; June 2002) helped to clarify a number of timing issues.

Guiding decisions

The final shape of the timing scheme has evolved gradually, following a number of "small steps", taken one after the other, with the consequences they implied. The crucial, guiding principle was the decision to distribute to the sub-detectors the **BC** clock of the *best "TTC quality", without any degradation* introduced by the adopted CPT/LTU structure. The "quality", in this case, means a *jitter* expected at the output of a correctly implemented TTCrx chip, a minimum long-term *drift* and a stable and fixed *LHC phase*. The three terms, frequently used in the text, have the following meaning:

LHC phase: the phase (0 to 25ns) of a clock or a signal *in respect to the real time of the LHC bunch crossing*; can only be evaluated indirectly.

Jitter: a cycle-to-cycle deviation of a clock or a signal edge from its average phase.

Drift: phase shift of a clock or a signal *in respect to the LHC bunch-crossing*; usually a long-term effect, caused by variations in temperature, power supply levels, changes of circuit propagation time, *etc.* ; likely to have a daily pattern.

Alternative schemes

The timing survey revealed that the majority of sub-detectors could tolerate a relatively large drift of the clock (1 to 2 ns) and are not affected by its LHC phase; some have an automated procedure to correct the LHC phase in case of a change; the sub-detectors with "special requirements" provide for themselves and are not affected by the "general solution". It was tempting, therefore, to at least evaluate the benefits of a different design approach that delivers the **BC** clock of reduced but still acceptable specification in exchange for a simplification to the synchronisation procedure and/or the improvement of the **L0/L1** latency.

In the "alternative" schemes that were considered, the ***BC** clock would be distributed to the sub-detector TTC partitions from the CTP*, together with the trigger signals and the data it

synchronises; the sub-detectors would never see any change in the relative timing, the TTC interface requirements would be automatically satisfied "by design" and would not ever require a re-adjustment. No significant deterioration of the **BC** jitter would be likely, but the drift would be higher since the clock propagates through the CTP system before reaching the sub-detectors; also, the LHC phase of the clock would change whenever the CTP timing is modified.

A possible reason for the re-adjustment of the CTP timing could be a major modification, or a mishap, but the most likely cause would be the "tracking" of the last-arriving among the **L0** trigger inputs, in order to reduce the overall **L0** trigger latency. In case of the "alternative scheme", the "tracking" might produce a surprising result: the delay of the CTP clock, in order to "catch early" an **L0** trigger input, would delay equally the **BC** clock delivered to the triggering sub-detector that is the source of the trigger input; as a result, if the trigger input is synchronised by the local sub-detector clock, it would also be delayed and the phase between the input signal and the re-adjusted CTP clock, the very reason for the whole operation, would remain unchanged. If, on the other hand, the trigger input has a fixed LHC phase - a very likely scenario, made possible by the corresponding re-adjustment, automatic or otherwise, of the local clock, the timing between the trigger input and the CTP clock could be easily set to the appropriate value.

Main features

The potential "tracking problem", associated with the "alternative schemes", and a prudent decision to deliver to the sub-detectors the **BC** clock of the best available quality - just in case, even if it exceeds the current requirements, led to the adoption of a design approach that shall result in the system with the following main features:

MF1 The LHC phase of the **BC** clock delivered to sub-detectors *shall remain fixed*; the long-term drift shall be very small - several hundreds of picoseconds; the expected jitter at the output from the TTCrx chip shall be around 80ps (rms).

MF2 With the LHC phase of the **BC** clock fixed, the LHC phase of the CTP trigger inputs (**L0, L1, L2**) shall also remain unchanged (short of major modifications or mishaps).

MF3 Any change of the LHC phase of the CTP **BC** clock shall require a rather complicated tuning of *all* 24 sub-detector TTC partitions. There shall be at least three critical delay adjustments in each partition that shall need to be individually set and verified.

MF4 The scheme achieves the *shortest possible* **L0** latency, but the LHC phase of the **L0** trigger signal shall change whenever the CTP timing is altered.

MF5 The LHC phase of the **L1** trigger, delivered *via* the TTC system, remains fixed, but the effective **L1** latency shall change whenever the CTP timing is re-adjusted; the difference between the maximum and the minimum **L1** latency shall not exceed two **BC** clock intervals - 50ns.

The term *latency* has been used for the delay between the last-arriving **L0/L1** trigger input to the CTP and the corresponding **L0/L1** signal delivered to the sub-detectors. The delay includes the propagation time through the CTP logic (with the 100ns limit explicitly set in the CTP URD), the propagation time through the LTU board and, in case of the **L1** signal, the transmission time through the TTC system (TTCex board, optical fibre, the TTCrx chip).