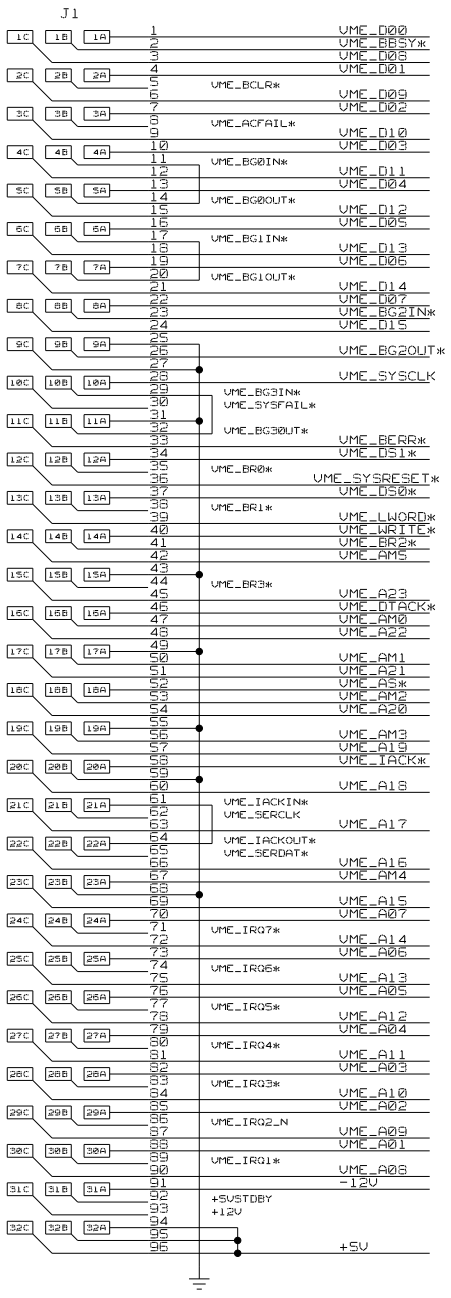
A | 2-TE-0119-001-01-B | THIS DRAWING CONFORMS TO B.S. 3939

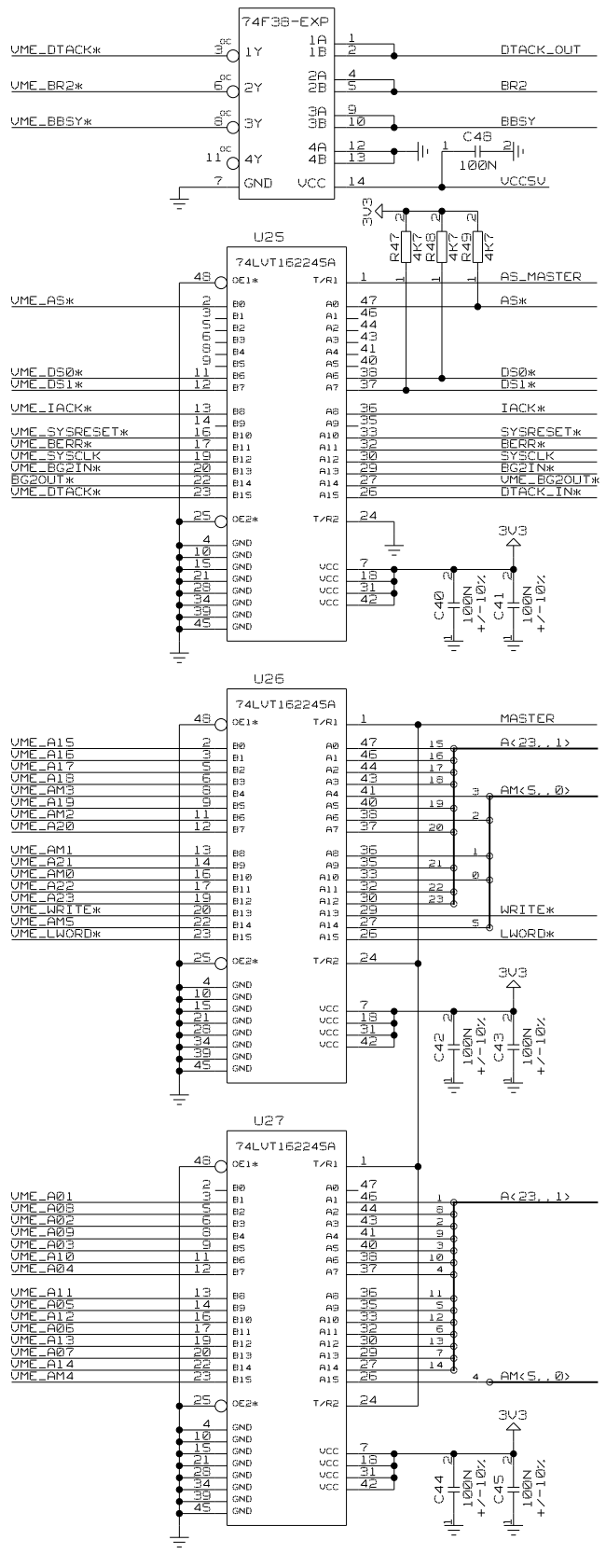
VME CONNECTIONS

VME J1 CONNECTIONS

PL-DIN41612-96

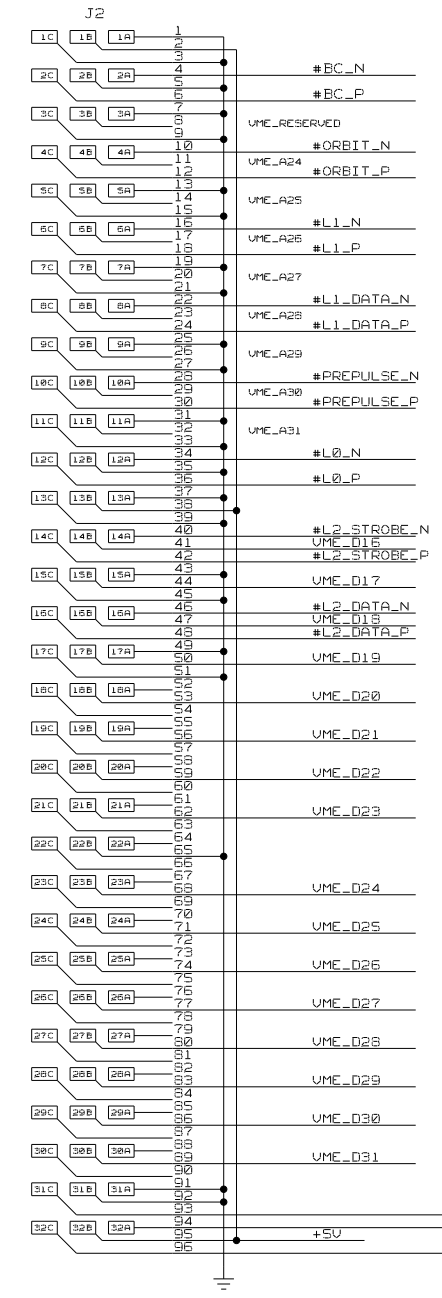


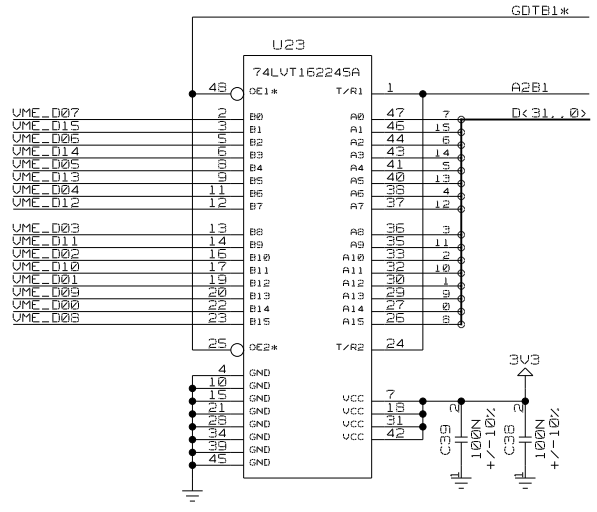
VME_BGXIN/OUT* AND VME_BR2*
TRACKS ON SOLDER SIDE

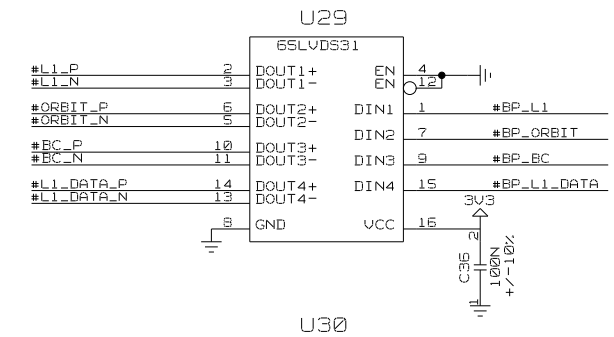


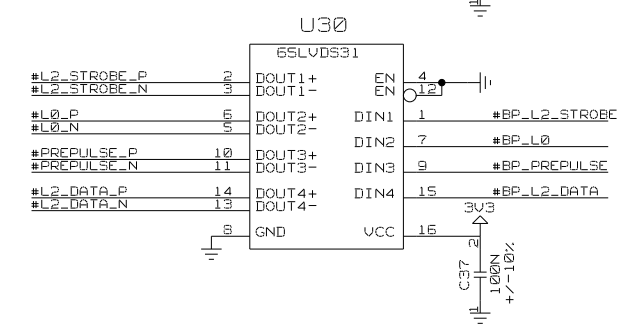
VME J2 CONNECTIONS

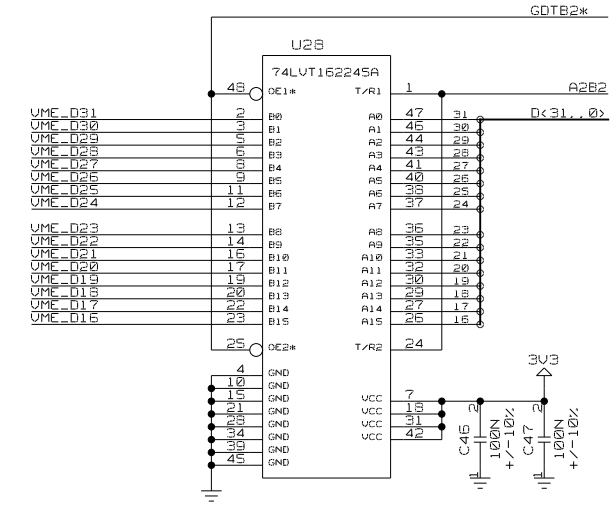
PL-DIN41612-96











I2C CONTROL BUS <SHEET 5>
SCL
GND/VDD
SDA

LTU FPGA <SHEET 4>

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	25-05-2004	TE245	P. JOVANOVIC	P. JOVANOVIC	P. JOVANOVIC	
A	15-12-2003	- - - - -	P. JOVANOVIC	P. JOVANOVIC	P. JOVANOVIC	

USED ON: ALICE CENTRAL TRIGGER PROCESSOR

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CCLRC
COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3265M CIRCUIT

LOCAL TRIGGER UNIT (LTU)

VME CONNECTIONS

A - 45/03
B - 37/04

A | 2-TE-0119-001-01-B

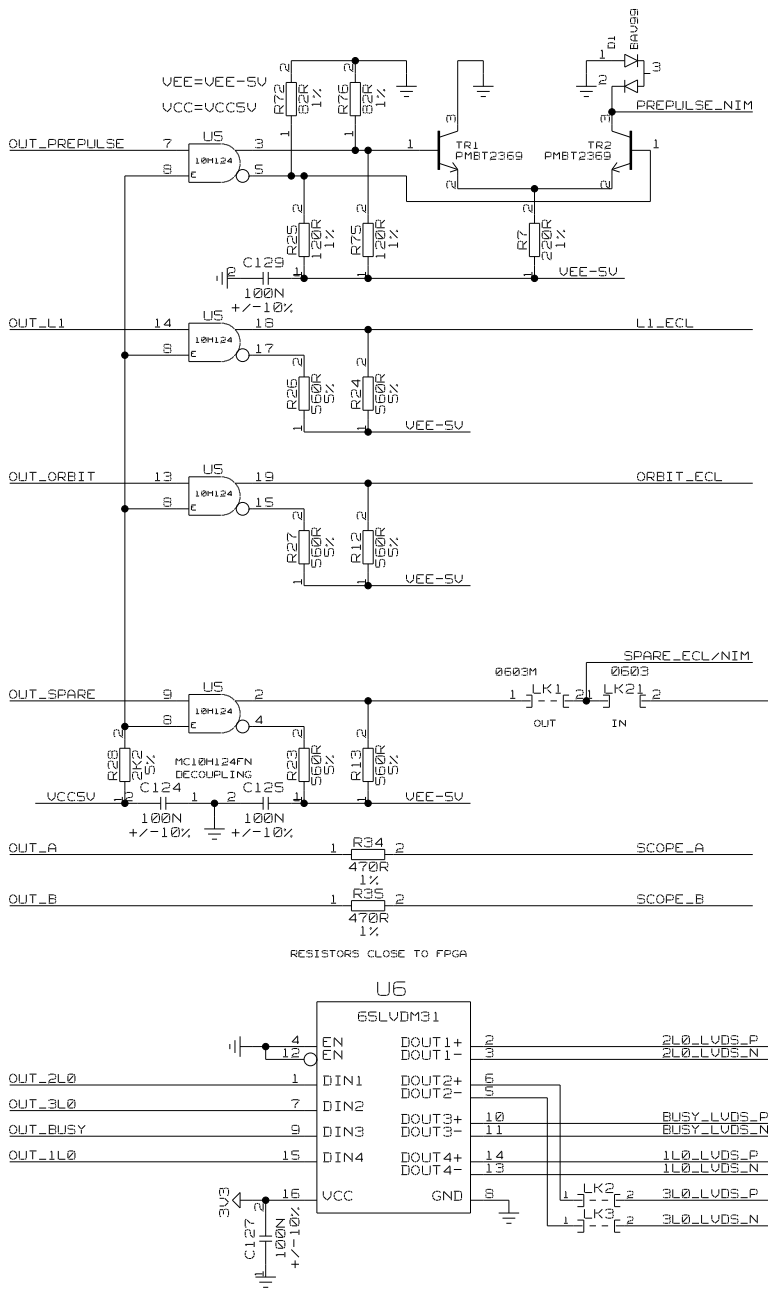
TOTAL NO. OF SHEETS 5

A | 2-TE-0119-001-01-B

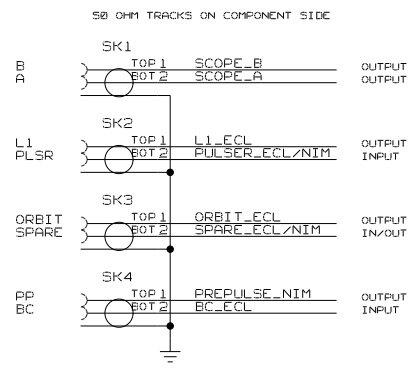
A | 2-TE-0119-001-02-B | THIS DRAWING CONFORMS TO B.S. 3939

FRONT PANEL CONNECTIONS

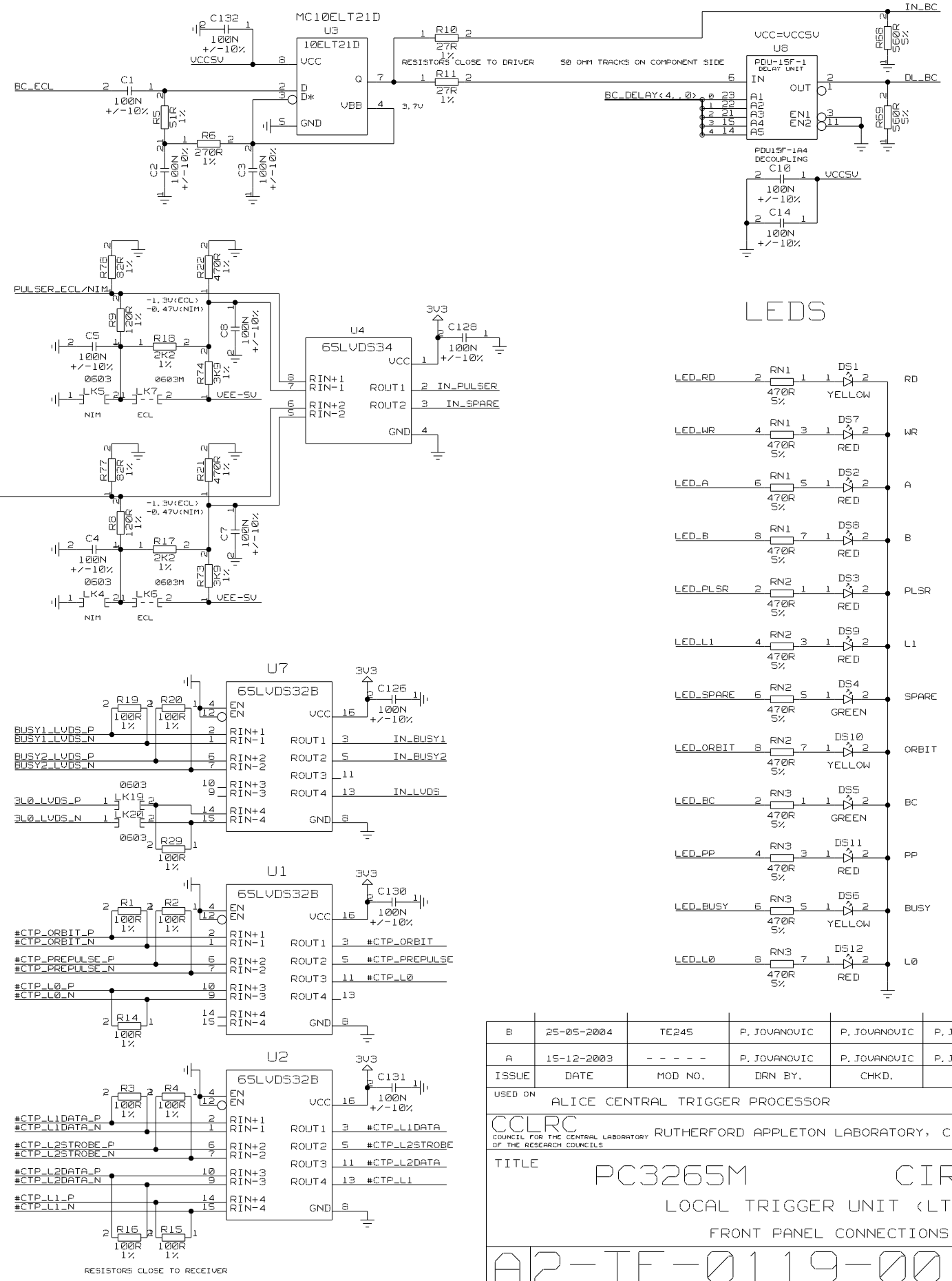
LTU OUTPUTS



CONNECTORS



LTU INPUTS



BC DELAY

LEDS

ALL THE INTERNAL SIGNALS CONNECTED TO THE LTU FPGA <SHEET 4>

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	25-05-2004	TE245	P. JOVANOVIC	P. JOVANOVIC	P. JOVANOVIC	
A	15-12-2003	- - - - -	P. JOVANOVIC	P. JOVANOVIC	P. JOVANOVIC	

USED ON: ALICE CENTRAL TRIGGER PROCESSOR

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RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3265M CIRCUIT

LOCAL TRIGGER UNIT (LTU)

FRONT PANEL CONNECTIONS

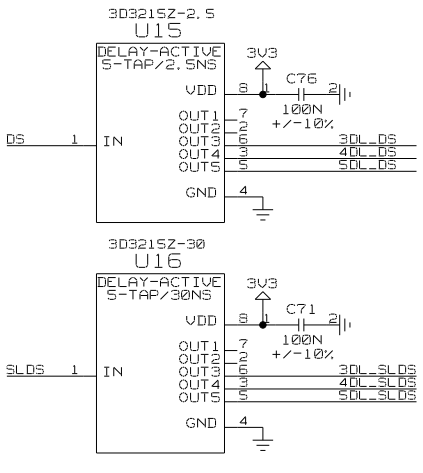
A - 45/03
B - 37/04

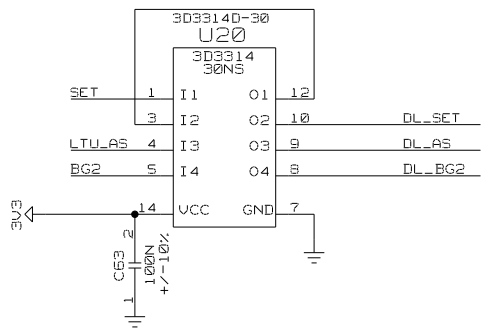
A | 2-TE-0119-001-02-B

TOTAL NO. OF SHEETS 5

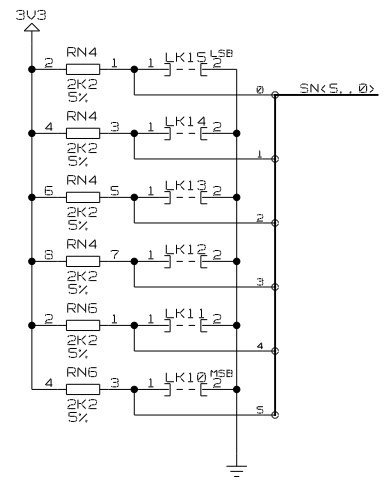
A 2-TE-0119-001-02-B

DELAY LINES

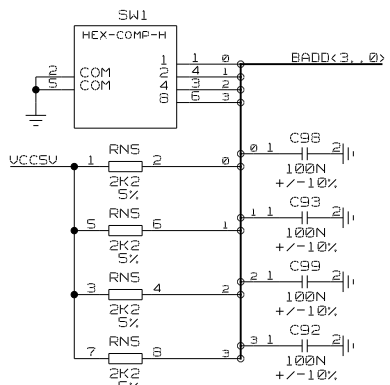




SERIAL NUMBER

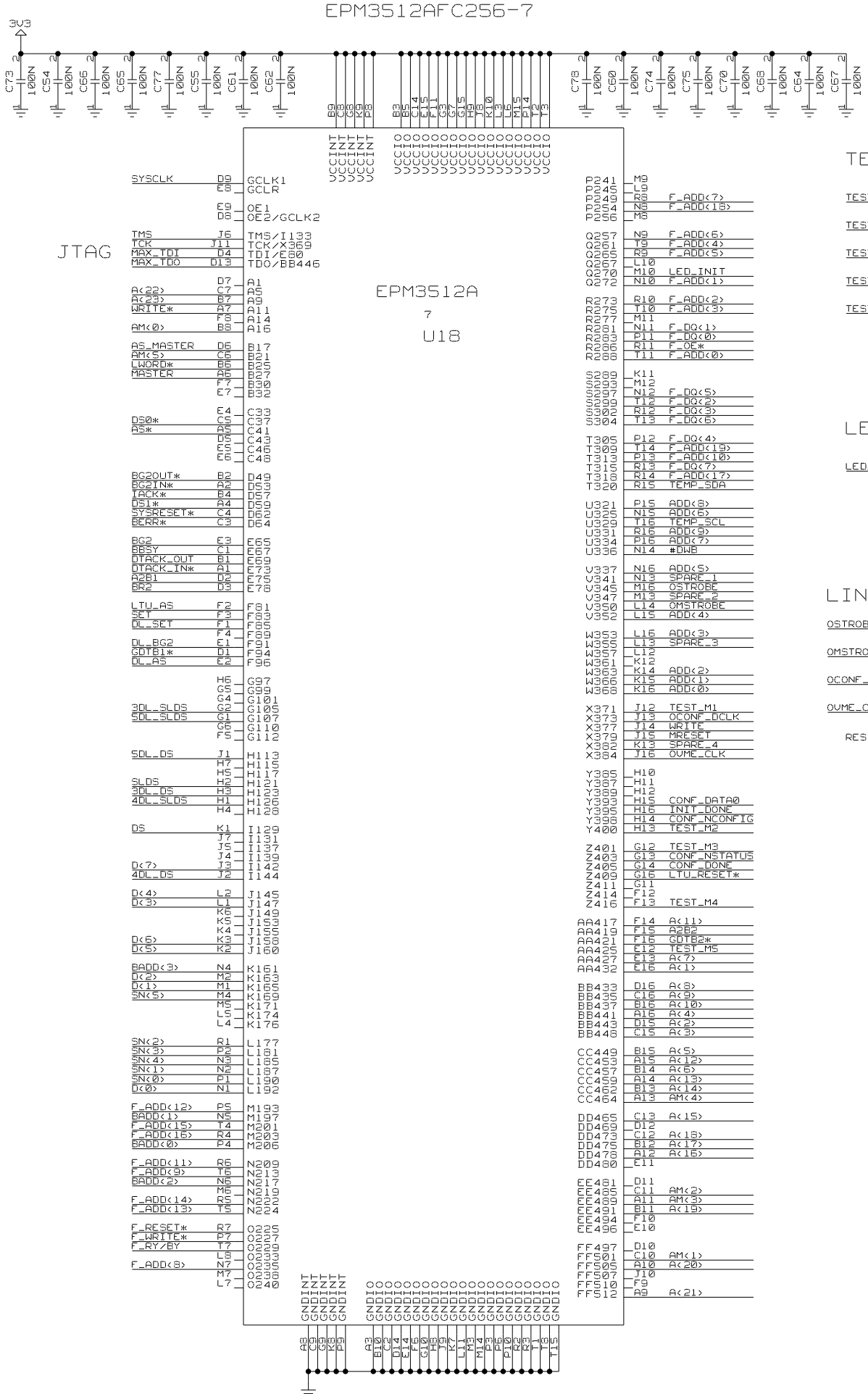


BOARD ADDRESS

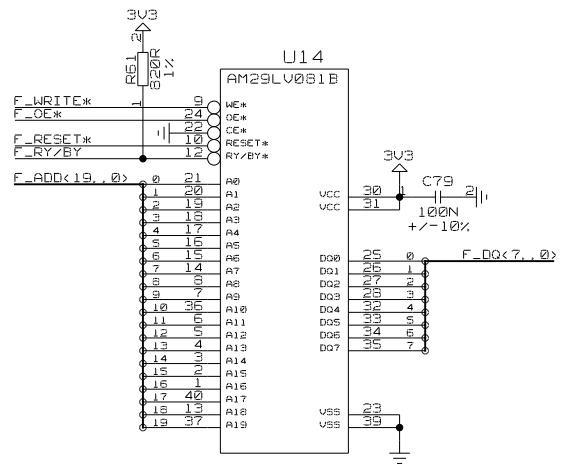


VME INTERFACE CONTROLLER

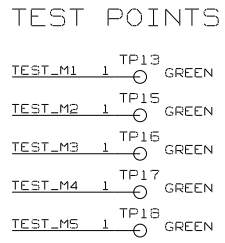
EPM3512AFC256-7



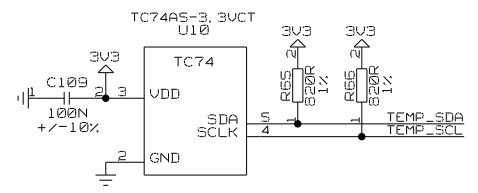
FLASH MEMORY



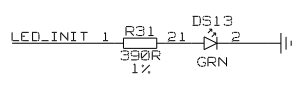
TEST POINTS



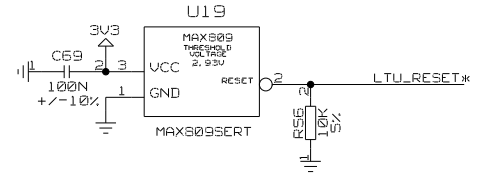
TEMPERATURE SENSOR



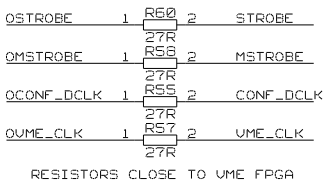
LED FPGA INIT.



POWER-ON RESET



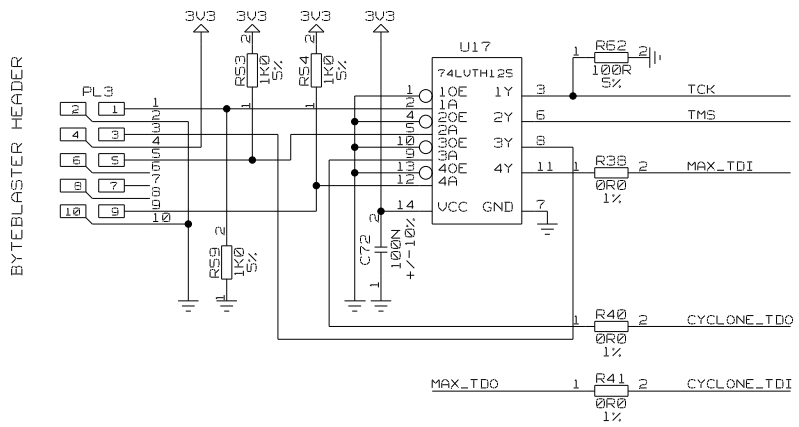
LINE TERMINATION



RESISTORS CLOSE TO VME FPGA

50 OHM TRACKS

JTAG CONNECTION



ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	25-05-2004	TE245	P. JOVANOVIC	P. JOVANOVIC	P. JOVANOVIC	
A	15-12-2003	- - - - -	P. JOVANOVIC	P. JOVANOVIC	P. JOVANOVIC	

USED ON: ALICE CENTRAL TRIGGER PROCESSOR

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RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3265M CIRCUIT

LOCAL TRIGGER UNIT (LTU)

VME INTERFACE CONTROLLER

A - 45/03
B - 37/04

A | 2-TE-0119-001-03-B

TOTAL NO. OF SHEETS 5

A	2-TE-0119-001-04-B	THIS DRAWING CONFORMS TO B.S. 3939

LTU LOGIC FPGA

EP1C12F324C7

U13 EP1C12 I/O BLOCK 1

#CTP_L0	D4	IO_VREF0B1	C14	IO_VREF0B2	ADD<1>
	H6	IO_VREF1B1	E10	IO_VREF1B2	
OUT_BUSY	R1	IO_VREF2B1	A6	IO_VREF2B2	OUT_B
ADC_CS*	P4	IO_1			
OUT_SPARE	M1	IO_2		IO_5	E11
	H1	IO_3		IO_6	E13
#CTP_L1DATA	D1	IO_4			
LED_BUSY	T3	IO_LVDS0N	G5	IO_LVDS25P	
IN_LVDS	T2	IO_LVDS0P	F5	IO_LVDS25N	
IN_BUSY2	R3	IO_LVDS1N	B4	IO_LVDS26P	SPARE_1
IN_BUSY1	R2	IO_LVDS1P	A4	IO_LVDS26N	OUT_A
OUT_SL0	P3	IO_LVDS2N	D5	IO_LVDS27P	LED_A
OUT_IL0	P2	IO_LVDS2P	C5	IO_LVDS27N	LED_RD
ADC_SDATA	N4	IO_LVDS3N	C6	IO_LVDS28P	LED_WR
ADC_CLK	N3	IO_LVDS3P	B6	IO_LVDS28N	D<5>
	N6	IO_LVDS4N	D6	IO_LVDS29P	LED_B
	N5	IO_LVDS4P	E6	IO_LVDS29N	TEST_C5
	N7	IO_LVDS5N	A7	IO_LVDS30P	D<5>
	M6	IO_LVDS5P	D7	IO_LVDS30N	
OUT_PREPULSE	N2	IO_LVDS6N	B7	IO_LVDS31P	D<10>
OUT_SL0	N1	IO_LVDS6P	A7	IO_LVDS31N	D<11>
ADC_IN	M4	IO_LVDS7N	E7	IO_LVDS32P	
	M5	IO_LVDS7P	E8	IO_LVDS32N	
OUT_ORBIT	M2	IO_LVDS8N	B8	IO_LVDS33P	D<14>
OUT_L1	M3	IO_LVDS8P	A8	IO_LVDS33N	D<15>
	L4	IO_LVDS9N	C8	IO_LVDS34P	D<13>
	L5	IO_LVDS9P	D8	IO_LVDS34N	D<12>
IN_SPARE	L3	IO_LVDS10N	E9	IO_LVDS35P	D<2>
IN_PULSER	L2	IO_LVDS10P	A9	IO_LVDS35N	D<3>
	L6	IO_LVDS11N	C9	IO_LVDS36P	D<1>
	L7	IO_LVDS11P	D9	IO_LVDS36N	D<0>
	H5	IO_LVDS12N	F9	IO_LVDS37P	
BC_DELAY<2>	H4	IO_LVDS12P	G9	IO_LVDS37N	
BC_DELAY<3>	H3	IO_LVDS13N	A10	IO_LVDS38P	D<7>
BC_DELAY<4>	H2	IO_LVDS13P	B10	IO_LVDS38N	D<6>
	G6	IO_LVDS14N	D10	IO_LVDS39P	D<4>
LED_LOCK	G5	IO_LVDS14P	C10	IO_LVDS39N	D<5>
TEST_C1	G4	IO_LVDS15N	E11	IO_LVDS40P	ADD<9>
LED_SPARE	G3	IO_LVDS15P	B11	IO_LVDS40N	ADD<8>
	F7	IO_LVDS16N	D11	IO_LVDS41P	ADD<6>
TEST_C3	F6	IO_LVDS16P	C11	IO_LVDS41N	ADD<7>
LED_FP	G2	IO_LVDS17N	A12	IO_LVDS42P	SPARE_2
LED_BC	G1	IO_LVDS17P	B12	IO_LVDS42N	SPARE_3
TEST_C2	F5	IO_LVDS18N	C12	IO_LVDS43P	ADD<5>
LED_L1	F4	IO_LVDS18P	D12	IO_LVDS43N	ADD<4>
LED_PLSR	F3	IO_LVDS19N	C13	IO_LVDS44P	ADD<3>
LED_ORBIT	F2	IO_LVDS19P	D13	IO_LVDS44N	ADD<2>
TEST_C4	E5	IO_LVDS20N	A13	IO_LVDS45P	STROBE
#CTP_PREPULSE	E4	IO_LVDS20P	B13	IO_LVDS45N	#DWB
#CTP_L2STROBE	E3	IO_LVDS21N	F10	IO_LVDS46P	
#CTP_L2DATA	E2	IO_LVDS21P	G10	IO_LVDS46N	
#CTP_L1	D3	IO_LVDS22N	D14	IO_LVDS47P	
#CTP_ORBIT	C2	IO_LVDS23N	C15	IO_LVDS47N	ADD<0>
	J5	VCCA_PLL1	A15	IO_LVDS48P	MSTROBE
BC_DELAY<0>	K5	IO_PLL1_OUTN	B15	IO_LVDS48N	SPARE_4
BC_DELAY<1>	K4	IO_PLL1_OUTP	F11	IO_LVDS49P	
	K1	GNDA_PLL1	G11	IO_LVDS49N	
	J6	GNDG_PLL1	B16	IO_LVDS50P	WRITE
			C16	IO_LVDS50N	MRESET
	P5	IO_DPCLK0			
IN_BC	F1	IO_DPCLK1		IO_DPCLK2	BS
			B14	IO_DPCLK3	VME_CLK
DL_BC	J3	CLK0_LVDSCLK1P			
	J4	CLK1_LVDSCLK1N			

ALTERA — BODY 1 OF 5

1V5 L1 2.2U

C18 10U +/-10% CASE-A; C105 100N +/-10%; C120 10N +/-10%

FPGA PLL DECOUPLING

U13 EP1C12 I/O BLOCK 2

LA_C3-6	E14	IO_VREF0B3	P13	IO_VREF0B4	
	J14	IO_VREF1B3	P9	IO_VREF1B4	
D<23>	P16	IO_VREF2B3	R5	IO_VREF2B4	
LA_CLOCK	D18	IO_7	P12	IO_12	
LA_A2-0	H15	IO_8	P10	IO_13	
	L14	IO_9			
D<16>	M16	IO_10			
D<22>	P17	IO_11			
LA_A3-7	D17	IO_LVDS51P	T15	IO_LVDS76N	SSH_A<8>
	C17	IO_LVDS51N	U16	IO_LVDS76P	D<31>
LA_C3-7	D15	IO_LVDS52P	M11	IO_LVDS77N	
	D16	IO_LVDS52N	N11	IO_LVDS77P	
LA_A3-6	E15	IO_LVDS53P	U15	IO_LVDS78N	SSH_A<9>
LA_C3-5	E16	IO_LVDS53N	V15	IO_LVDS78P	SSH_A<10>
LA_A3-4	F15	IO_LVDS54P	R14	IO_LVDS79N	TEST_C6
LA_A3-3	F16	IO_LVDS54N	T14	IO_LVDS79P	SSH_DQ<16>
LA_C3-4	F14	IO_LVDS55P	M10	IO_LVDS80N	
	F13	IO_LVDS55N	N10	IO_LVDS80P	
LA_A3-2	F17	IO_LVDS56P	R13	IO_LVDS81N	SSH_DQ<0>
LA_A3-1	F18	IO_LVDS56N	T13	IO_LVDS81P	SSH_DQ<1>
	F12	IO_LVDS57P	U13	IO_LVDS82N	SSH_A<11>
	G12	IO_LVDS57N	V13	IO_LVDS82P	SSH_A<12>
LA_A2-5	G16	IO_LVDS58P	R12	IO_LVDS83N	SSH_DQ<2>
LA_A2-7	G15	IO_LVDS58N	T12	IO_LVDS83P	SSH_DQ<3>
LA_A2-0	G14	IO_LVDS59P	U12	IO_LVDS84N	SSH_A<13>
	G13	IO_LVDS59N	V12	IO_LVDS84P	SSH_A<14>
LA_A2-5	G17	IO_LVDS60P	V11	IO_LVDS85N	SSH_WRITE*
LA_A2-4	G18	IO_LVDS60N	U11	IO_LVDS85P	SSH_A<15>
LA_A2-1	H17	IO_LVDS61P	T11	IO_LVDS86N	SSH_DQ<5>
LA_A2-3	H16	IO_LVDS61N	R11	IO_LVDS86P	SSH_DQ<4>
LA_A2-2	H15	IO_LVDS62P	R10	IO_LVDS87N	SSH_DQ<6>
	H14	IO_LVDS62N	T10	IO_LVDS87P	SSH_DQ<7>
	H13	IO_LVDS63P	U10	IO_LVDS88N	SSH_CLK
	J13	IO_LVDS63N	V10	IO_LVDS88P	SSH_A<16>
#BP_PREPULSE	L15	IO_LVDS64P	N9	IO_LVDS89N	
#BP_L0	L16	IO_LVDS64N	M9	IO_LVDS89P	
	L13	IO_LVDS65P	T9	IO_LVDS90N	SSH_A<17>
	M13	IO_LVDS65N	R9	IO_LVDS90P	SSH_DQ<17>
#BP_L1_DATA	L17	IO_LVDS66P	V9	IO_LVDS91N	SSH_A<18>
OBP_BC	L18	IO_LVDS66N	U9	IO_LVDS91P	SSH_A<19>
D<17>	M15	IO_LVDS67P	R8	IO_LVDS92N	SSH_DQ<9>
	M14	IO_LVDS67N	T8	IO_LVDS92P	SSH_DQ<8>
#BP_L2_DATA	M17	IO_LVDS68P	V8	IO_LVDS93N	SSH_A<0>
#BP_L2_STROBE	M18	IO_LVDS68N	U8	IO_LVDS93P	SSH_A<1>
D<21>	N15	IO_LVDS69P	R7	IO_LVDS94N	SSH_DQ<11>
D<20>	N16	IO_LVDS69N	T7	IO_LVDS94P	SSH_DQ<10>
	N12	IO_LVDS70P	V7	IO_LVDS95N	SSH_A<2>
	N13	IO_LVDS70N	U7	IO_LVDS95P	SSH_A<3>
D<19>	N17	IO_LVDS71P	R6	IO_LVDS96N	SSH_DQ<13>
D<18>	N18	IO_LVDS71N	T6	IO_LVDS96P	SSH_DQ<12>
TEST_C5	N14	IO_LVDS72P	P7	IO_LVDS97N	
TEST_C7	P14	IO_LVDS72N	P6	IO_LVDS97P	
D<27>	R16	IO_LVDS73P	U6	IO_LVDS98N	SSH_A<5>
D<28>	R15	IO_LVDS73N	V6	IO_LVDS98P	SSH_A<4>
D<25>	R18	IO_LVDS74P	U5	IO_LVDS99N	SSH_CE*
D<26>	R17	IO_LVDS74N	T5	IO_LVDS99P	SSH_DQ<14>
D<29>	T17	IO_LVDS75P	U4	IO_LVDS100N	SSH_A<7>
D<30>	T16	IO_LVDS75N	T4	IO_LVDS100P	SSH_DQ<15>
	J12	VCCA_PLL2	N8	IO_LVDS101N	
#BP_ORBIT	K15	IO_PLL2_OUTP	M8	IO_LVDS101P	
#BP_L1	K16	IO_PLL2_OUTN	V4	IO_LVDS102N	SSH_A<6>
	K17	GNDA_PLL2	U3	IO_LVDS102P	LED_L0
	J18	GNDG_PLL2			
LA_A3-5	E17	IO_DPCLK4	U14	IO_DPCLK6	
D<24>	P15	IO_DPCLK5	R4	IO_DPCLK7	
	J15	CLK2_LVDSCLK2P			
	J16	CLK3_LVDSCLK2N			

ALTERA — BODY 2 OF 5

1V5 C91 100N

SNAP-SHOT MEMORY

TEST POINTS

TEST_C1	TP2	GREEN
TEST_C2	TP3	GREEN
TEST_C3	TP4	GREEN
TEST_C4	TP5	GREEN
TEST_C5	TP6	GREEN
TEST_C6	TP11	GREEN
TEST_C7	TP12	GREEN
TEST_C8	TP14	GREEN

PLL LOCK LED

LED_LOCK — R32 390R 1% — DS14 GRN

LINE TERMINATION

OBP_BC — R37 27R 1% — #BP_BC

RESISTOR CLOSE TO FPGA

50 OHM TRACKS

C101–C110 100N; C111 10N; C112 100N

U12 CY7C1382B 133AI

	15	VDD			
	41	VDD			
	65	VDD			
	91	VDD			
	4	VDDQ			
	11	VDDQ			
	20	VDDQ			
	27	VDDQ			
	54	VDDQ			
	61	VDDQ			
	70	VDDQ			
	77	VDDQ			
SSH_CLK	89	CLK			
	88	ADV*			
	85	ADSC*			
	84	ADSP*			
SSH_A<19..0>	37	A0			
	36	A1			
	35	A2			
	34	A3			
	33	A4			
	32	A5			
	100	A6			
	99	A7	DQA0	73	SSH_DQ<17..0>
	50	A8	DQA1	72	
	81	A9	DQA2	69	
	80	A10	DQA3	68	
	49	A11	DQA4	3	
	48	A12	DQA5	2	
	47	A13	DQA6	95	
	46	A14	DQA7	94	
	45	A15	DQB0	23	
	44	A16	DQB1	22	
	43	A17	DQB2	19	
	42	A19	DQB3	18	
			DQB4	13	
			DQB5	12	
			DQB6	9	
			DQB7	8	
SSH_CE*	98	CE1*	DPA	74	
	97	CE2	DPB	24	
SSH_WRITE*	92	CE3*			
	93	GW*			
	87	OE*			
	94	BWE*			
	31	BWSA*			
	64	BWSB*			
	14	MODE			
	17	ZZ			
	5	VSS			
	10	VSS			
	21	VSS			
	26	VSS			
	40	VSS			
	55	VSS			
	60	VSS			
	67	VSS			
	71	VSS			
	76	VSS			
	90	VSS			

CYPRESS TQFP

CY7C1382B-133AC

ADC

ADC_IN — R71 1K0 1% — C122 100N +/-10%; C119 10U +/-10%

U9 LTC1096L: VCC, VREF, DOUT, IN-, IN+, CS/SHUTDOWN, CLK, GND

R70 10R 1%; C15 0805 1U +/-10%; C121 100N +/-10%

ADC_CS* / ADC_CLK

ADC_SDATA

ADD LTC1096LCS8

FPGA CONFIGURING

U13 EP1C12 CONFIG BLOCK

CONF_DCLK	L1	DCLK	ASDO	K6	
	D3	CLKUSR	CEO*	K2	
3V3	K7	MSEL1	CSO*	J1	
	K3	MSEL0	INIT_DONE	C3	INIT_DONE
CONF_NCONFIG	J7	CE*	STATUS*	L12	CONF_NSTATUS
	J2	CONFIG*	CONF_DONE	K17	CONF_DONE
CONF_DATA0	H7	DATA0			
	C4	DEV_CLR			
	B3	DEV_OE			

ALTERA — BODY 4 OF 5

R36 4K7 5%; R63 4K7 5%; R67 4K7 5%

FPGA JTAG CONNECTIONS

U13 EP1C12 JTAG BLOCK

CYCLONE_TDI	J17	TDI	TDO	K13	CYCLONE_TDO
TMS	K14	TMS			
TCK	K18	TCK			

ALTERA — BODY 3 OF 5

FPGA SUPPLY AND DECOUPLING

U13 EP1C12 POWER BLOCK

	A17	VCCINT	GND	A1	
	A2	VCCINT	GND	A16	
	B1	VCCINT	GND	A3	
	B18	VCCINT	GND	B17	
	H10	VCCINT	GND	B2	
	J9	VCCINT	GND	C1	
	K10	VCCINT	GND	C18	
	L9	VCCINT	GND	H11	
	U1	VCCINT	GND	H8	
	U18	VCCINT	GND	H9	
	V17	VCCINT	GND	J10	
	V2	VCCINT	GND	J11	
	E1	VCCIO1	GND	J8	
	G7	VCCIO1	GND	K11	
	M7	VCCIO1	GND	K8	
	P1	VCCIO1	GND	K9	
	A14	VCCIO2	GND	L10	
	A5	VCCIO2	GND	L11	
	E12	VCCIO2	GND	L8	
	E8	VCCIO2	GND	T1	
	E18	VCCIO3	GND	T18	
	M12	VCCIO3	GND	U17	
	M18	VCCIO3	GND	U2	
	P18	VCCIO3	GND	V1	
	P11	VCCIO4	GND	V16	
	P8	VCCIO4	GND	V18	
	V14	VCCIO4	GND	V3	
	V5	VCCIO4			

ALTERA — BODY 5 OF 5

C113, C118, C80, C114, C81, C85, C89, C115, C106, C82, C107, C116 — C84, C95, C96, C103, C104, C119, C102, C105, C94, C90, C83, C97 — 100N

LOGIC ANALYZER CONNECTION

PL-MICTOR-SMD-38

PL2

	1	2	
	3	4	
LA_CLOCK	5	6	
LA_A3-7	7	8	
LA_A3-6	9	10	
LA_A3-5	11	12	
LA_C3-5	13	14	
LA_A3-4	15	16	
LA_C3-4	17	18	
LA_A3-3	19	20	
LA_A3-2	21	22	
LA_A3-1	23	24	
LA_A3-0	25	26	
LA_A2-7	27	28	
LA_A2-6	29	30	
LA_A2-5	31	32	
LA_A2-4	33	34	
LA_A2-3	35	36	
LA_A2-2	37	38	
LA_A2-1			
LA_A2-0			

AMP/TYCO 2-767004-2

B	25-05-2004	TE245	P. JOVANOVIC	P. JOVANOVIC	P. JOVANOVIC	
A	15-12-2003	- - - - -	P. JOVANOVIC	P. JOVANOVIC	P. JOVANOVIC	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON: ALICE CENTRAL TRIGGER PROCESSOR

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RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3265M CIRCUIT

LOCAL TRIGGER UNIT (LTU)

LTU FPGA CONNECTIONS

A - 45/03
B - 37/04

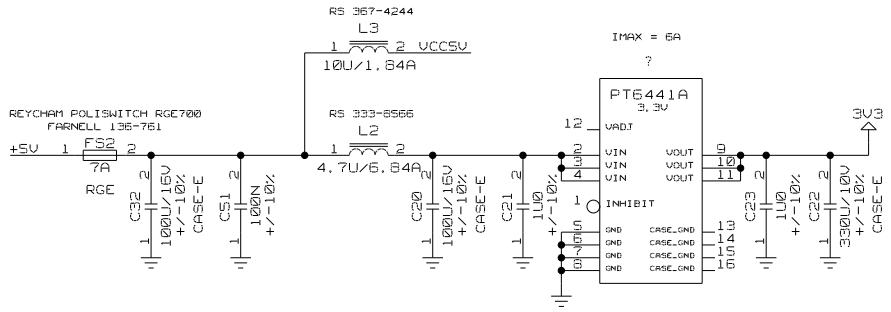
A 2-TE-0119-001-04-B

TOTAL NO. OF SHEETS 5

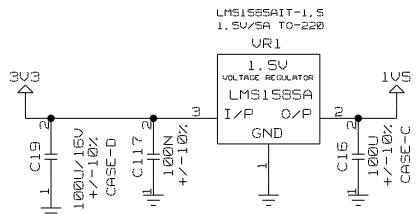
A	2-TE-0119-001-05-B	THIS DRAWING CONFORMS TO B.S. 3939

+5V CONNECTION

3V3 DC-DC CONVERTOR

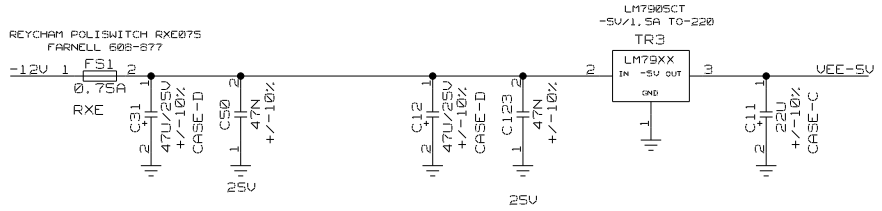


1.5V REGULATOR

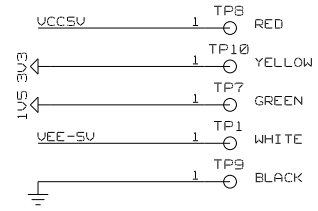


-12V CONNECTION

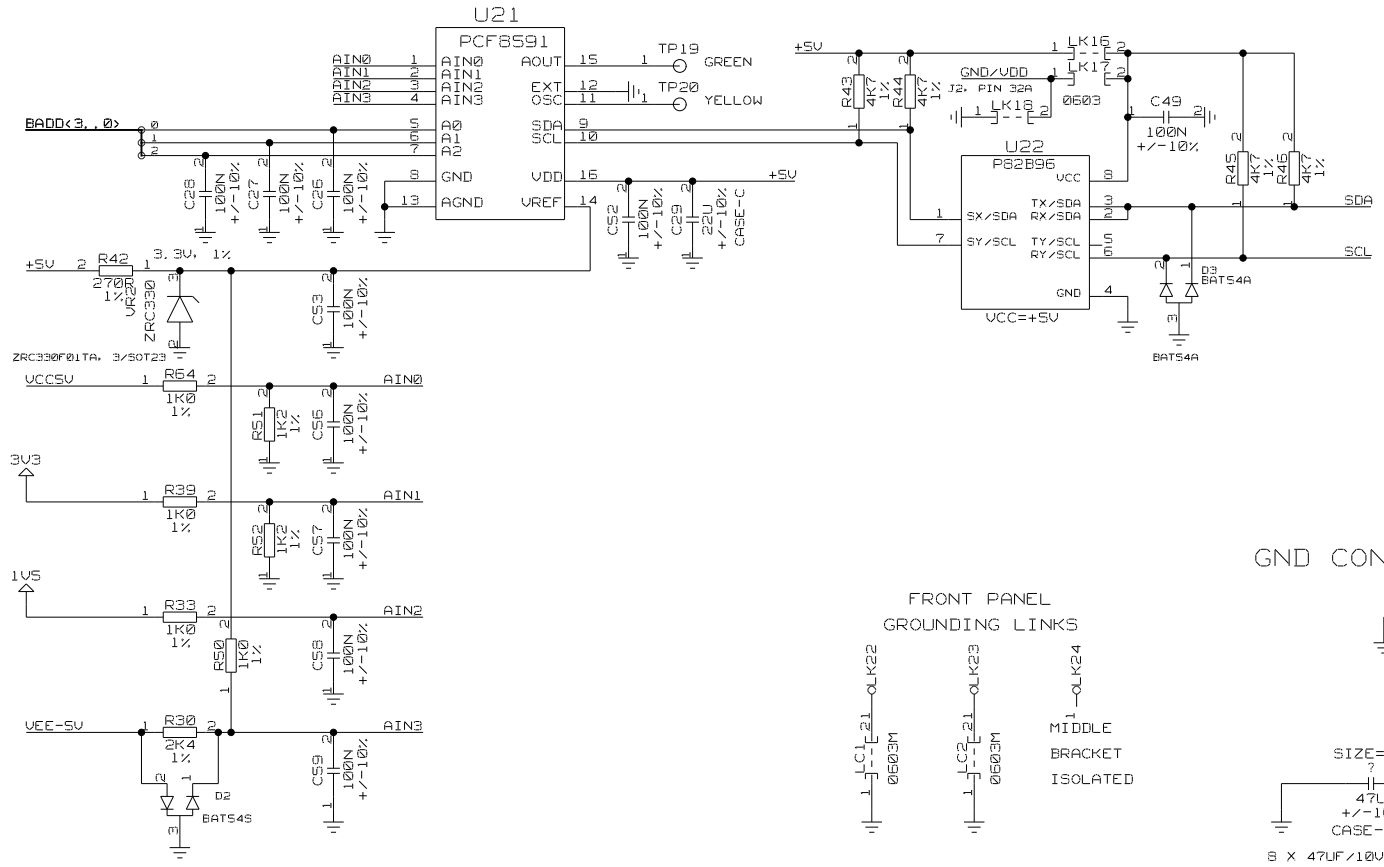
-5V REGULATOR



TEST POINTS

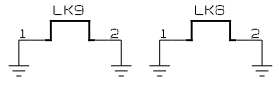


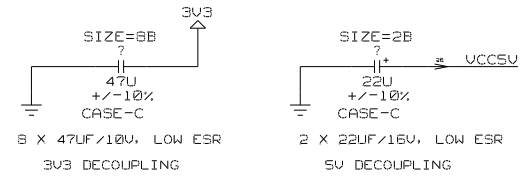
CONTROL - ADC AND THE I2C BUFFER



FRONT PANEL GROUNDING LINKS

GND CONNECTION FOR PROBES





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USED ON: ALICE CENTRAL TRIGGER PROCESSOR

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TITLE

PC3265M CIRCUIT

LOCAL TRIGGER UNIT (LTU)

POWER SUPPLY AND CONTROL

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B - 37/04

A 2-TE-0119-001-05-B

TOTAL NO. OF SHEETS 5