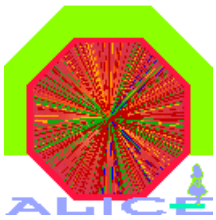

Layout and connections of the ALICE trigger system

PROPOSAL

Abstract:

This document proposes a *centralised* layout of the ALICE trigger system that offers considerable advantages over the *distributed* scheme, assumed during the debate on the CTP requirements.

The layout affects the detailed design of both the CTP and the sub-detector readout electronics, tasks that are already in progress. A decision about the final system architecture is *urgently* required.

The document discusses advantages and disadvantages of the proposed scheme and contains the plan of action, leading to the approval by the ALICE Technical Board.

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1.0 INTRODUCTION

1.1 Purpose and scope of the document

This is a *working* document, currently in a draft form. Comments and suggestions from the ALICE community are invited and encouraged.

The document is a *proposal,* intended to start a discussion among the experts and all the interested parties, leading, eventually, to the decision about the *final* structure and the layout of the ALICE trigger system.

A decision is urgently required since it affects the specification and the design of both the Central Trigger Processor [1] and the sub-detector readout electronics, tasks already in progress.

1.2 Document overview

The present section (***Introduction***) gives a brief account of the purpose and scope of the document, explains its structure, defines terms and acronyms and lists cited documents. The following section (***Proposal***) reviews the advantages and disadvantages of different options, sets out the details of the new proposal for the layout and connections of the ALICE trigger system, and stresses the need for urgent decision.

1.3 Acknowledgement

The ALICE detector uses the RD12 Timing Trigger and Control system (TTC) [2] [3] to synchronise the experiment with the LHC machine and to distribute the trigger signals from the CTP to the sub-detector readout electronics. Although a wealth of documentation is available on the TTC Web site [3], we greatly benefited from expertly advice, prompt response and generous help received on numerous occasions from the system guru, Bruce Taylor (CERN).

We are also grateful to Per Gällnö (CERN), the designer of the TTCvi, who accepted to modify the board (designer's nightmare) for the ALICE application with no fuss and in the shortest of time.

1.4 Definitions and acronyms

BC Bunch Crossing (clock) - the 40.08 MHz clock, locked to the LHC machine cycle, used to synchronise the pipeline processing system.

BUSY Signal formed by a sub-detector to indicate that it cannot accept another **L0** trigger.

CTP Central Trigger Processor [1] - electronic system that receives inputs from ALICE trigger sub-detectors and generates, in each bunch crossing, **L0**, **L1** and **L2** yes/no trigger decisions for all sub-detectors.

L0 Level-0 trigger (signal).

L1 Level-1 trigger (signal).

LTC Local Trigger Crate - a VME crate, part of the sub-detector electronics; contains the local system processor, the LTU, the TTC boards *etc*. .

LTU Local Trigger Unit (board).

RoI Region of Interest (option, logic, data).

TTC Timing, Trigger and Control (system) [2][3].

TTCcf TTC Clock Fanout (board) [8].

TTCex TTC Encoder/Transmitter (board) [9].

TTCit TTC Interface Test (board) [11].

TTCmi TTC Machine Interface (system, crate) [8].

TTCrx Timing, Trigger and Control Receiver ASIC [6].

TTCtx TTC Transmitter (board) [9].

TTCvi TTC -VMEbus Interface (board) [10].

U Unit of height in the standard 19" rack (1U = 1¾").

1.5 References

[1] *ALICE Central Trigger Processor: User Requirement Document,* current version available on the ALICE CTP web site [7].

[2] B.G. Taylor, *TTC Distribution for LHC Detectors*, IEEE Trans. Nuclear Science, Vol. 45, June 1998, pp. 821-828.

B.G. Taylor, *LHC Machine Timing Distribution for the Experiments*, Proceedings of the Sixth Workshop on Electronics for LHC Experiments, Crakow, Poland, 11-15 September 2000, pp.312-317.

[3] TTC web site: http://www.cern.ch/TTC/intro.html.

[4] *Conclusions and Afterthoughts,* available on the ALICE CTP web site [7].

[5] B.G. Taylor, CERN, private communication, February 2001.

[6] J. Christiansen et al., *TTCrx Reference Manual*, current version available on the TTC web site [3].

[7] ALICE CTP web site: (ALICE→Projects→Trigger), or, directly, http://www.ep.ph.bham.ac.uk/user/pedja/alice/.

[8] B.G. Taylor, *TTC Machine Interface (TTCmi) User Manual*, current version available on the TTC web site [3].

[9] B.G. Taylor, *Laser Transmitter Modules for TTC Distribution at the LHC Experiments*, current version available on the TTC web site [3].

[10] Ph. Farthouat et al., *TTC-VMEbus Interface (TTCvi-MkII),* current version available on the TTC web site [3].

[11] *TTC Interface Test Board (TTCit): Preliminary Specification,* available on the ALICE CTP web site [7].

2.0 PROPOSAL

2.1 Motivation

The current version of the CTP URD [1] provides a blueprint for the detailed design of the ALICE Central Trigger Processor. The document, developed with the participation of the whole ALICE trigger community, went through a number of revisions and is now pending the final approval of the Technical Board.

The other essential part of the ALICE trigger is the RD12 TTC system [2][3]. The TTC is used to synchronise the experiment with the LHC machine and to distribute trigger signals from the CTP to the sub-detector readout electronics. The design and the development of the system have been completed, the performance thoroughly tested and most of the components are already being produced; comprehensive documentation is available on the Web [3].

The detailed design of the CTP is about to start. Most design inputs appear to be defined, but the final layout and the connections of the trigger system are still uncertain. The system architecture also affects the design of the sub-detector readout electronics, the task that is already in progress.

The issue has been discussed in the past, but only in the background; it's now time to give it full attention in order to reach soon an agreed decision and the necessary approval of the Technical Board. The aim of this document is to help start the process.

2.2 Layout of the trigger system

2.2.1 *Sub-detector TTC partition*

The sub-detector TTC partition is shown in **Figure 1**. It consists of three VME boards: the LTU, the TTCvi and the TTCex. The TTCvi and the TTCex are developed by the RD12 collaboration; their full documentation is available on the TTC Web site [3].

The *Local Trigger Unit* (LTU) is the interface between the CTP and the sub-detector readout electronics, with the main function to enable the sub-detectors to operate in *stand-alone mode*. More information could be found in the CTP URD ([1], section ***Transmission of the trigger inputs***). The LTU's Preliminary Specification is being developed right now; it will be affected by the adopted layout of the ALICE trigger system.

For the sub-detectors that participate in the Region of Interest option, an additional board might be required - the RoI Interface. The option and its interface are not yet fully defined.

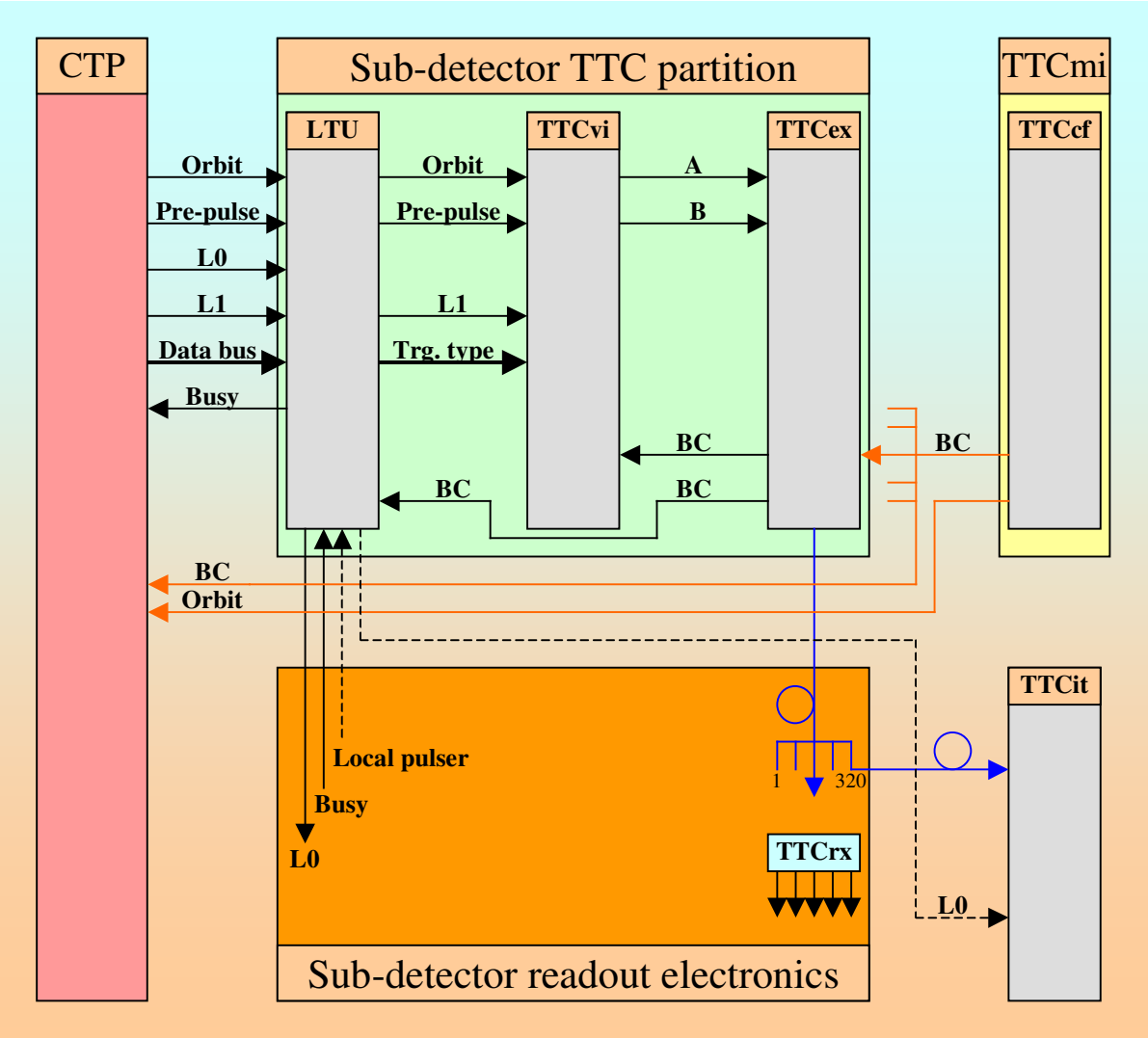

Figure 1 Connections of the sub-detector TTC partition and the readout electronics

2.2.2 *Current scheme - distributed layout*

In the discussions so far, it has been assumed that the sub-detector TTC partitions shall be *distributed*, as part of the local sub-detector electronics, residing in the *Local System Crates* (LSC). The notion of the LSC was introduced some time ago ([4], section 15); the name has recently been changed to *Local Trigger Crate* (LTC), defined as "a VME crate, part of the sub-detector electronics, contains the local system processor, the LTU, the TTC boards *etc*." ([1], section1.5). The feasibility of the scheme had been checked, but, until recently, no detailed analysis of the implementation had been attempted.

The main feature of the scheme is that all parts of the sub-detector dedicated electronics "travel" with the system and can be used independently of the CTP, at remote sites, or at times when the CTP is either not available or not required.

The overall system would require as many LTCs (VME crates) and as many local processors (VME processors) as there are sub-detectors in the ALICE experiment (20, according to the current version of the CTP URD - see [1], requirement 1.1.1).

In recent consultation with the TTC experts [5], we have been warned that a relatively long distance (20 - 50 m) between the ALICE TTC Machine Interface and the sub-detector TTC partitions is likely to cause a substantial increase in the BC clock jitter. The problem could be solved by distributing the clock optically and adding opto-electrical converters to the TTC partitions.

2.2.3 *New proposal - centralised layout*

The proposed layout of the ALICE trigger system is shown in **Figure 2**. The main difference in comparison with the "current scheme" (see the previous section) is that all the sub-detector TTC partitions shall be *centrally* located, installed in a number of VME crates, in racks adjacent to the rack with the CTP and the ALICE TTC Machine Interface (TTCmi). (The RoI fanout electronics, or the entire RoI system, could also be mounted in the rack.)

Each VME crate (21 slots) shall accommodate at least 4 TTC partitions (3 boards per partition; 4, if the RoI interface is also required); each crate shall have its own processor. For the maximum number of 20 sub-detectors (see [1], requirement 1.1.1), the total of 5 VME crates would be required. The system is scalable - the crates would be added as the number of ALICE sub-detector increases.

The electrical connections between the CTP and sub-detector TTC partitions are represented with arrows in **Figure 2**; more details are given in **Figure 1** and the full signal description can be found in [1]. In the proposed scheme, the length of the connections is only a metre or so. The critical length of cables distributing the **BC** clock from the TTCcf board in the ALICE TTC Machine Interface crate (TTCmi) is also reduced to a practical minimum.

The sub-detector readout electronics is located in the experimental cavern, 20 to 50 metres away from the CTP rack. The only electrical connections are the **L0** signal (50**Ω** coaxial cable; low propagation delay required in critical cases) and the **BUSY** input (signal level not yet defined). All the other trigger outputs from the CTP are transmitted over the TTC optical fibre (50/125 μm graded index multimode fibre, 1310 nm, propagation delay 4.9 ns/m). Each of the 10 identical optical outputs of the TTCex board can be locally fanned out by a passive *1:32 optical tree coupler* [3] to a total of 320 possible destinations. The number could be further increased by the addition of a TTCtx board to the sub-detector TTC partition.

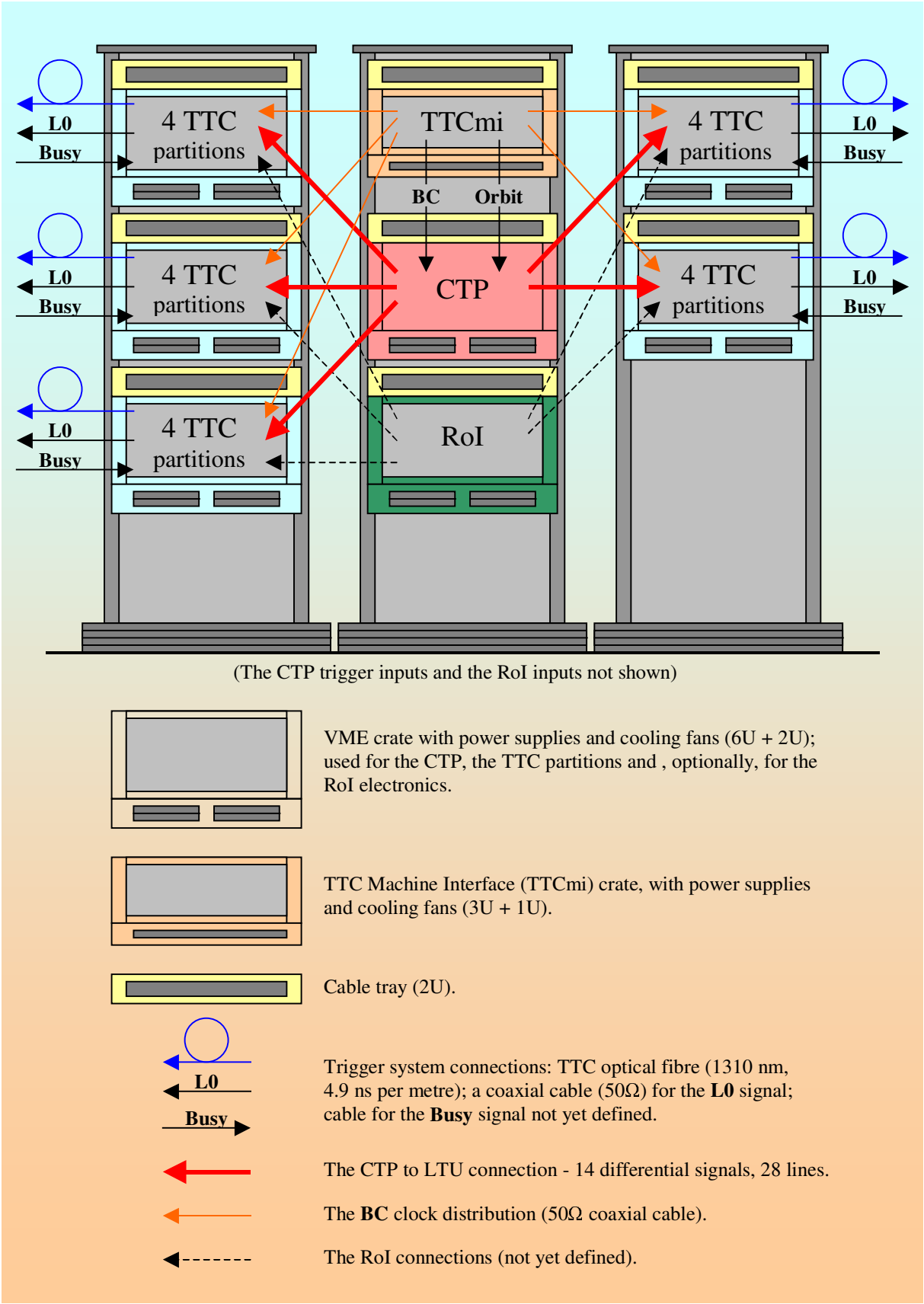

Figure 2 Layout and connections of the ALICE trigger system - *proposal*

At the sub-detector front-end electronics, the optical outputs are "de-multiplexed" by the TTCrx ASIC [6]. The circuit also "recovers" the **BC** clock, with the jitter estimated at around 80 ps rms. The sub-detectors that need a lower jitter could be provided with either a dedicated electrical output (jitter of only 7ps rms, but a long cable could increase it significantly - see the previous section); or a dedicated optical signal with a similar, low jitter, in which case a local opto-electrical converter would be required (example: AMP269050-1; PECL output; ~ 80 CHF [5]).

The TTCit board is foreseen as an optional debugging and monitoring tool. It could be added, temporarily or permanently, to the sub-detector TTC partition. It could also be installed separately, in Personnel Accessible Areas for example, for monitoring of the TTC operation during the physics run. The board requires only a single TTC optical channel; the dedicated L0 input is optional.

2.3 Advantages and disadvantages

Length of electrical connections

In case of the centralised layout, the length of electrical connections between the CTP and the sub-detector TTC partitions is reduced to a practical minimum. It improves the system reliability, diminishes the transmission error rate and eliminates a potential source of system noise.

The **BC** clock distribution network is also reduced to a minimum, which improves clock stability and eliminates another potential source of system noise (40 MHz signal).

Reduction of hardware

In case of the centralised layout, the number of VME crates and VME processors dedicated to the trigger operation would be reduced by at least 75% since, instead of up to 20 LTCs, only 5 (or less) crates are required to accommodate all the sub-detector TTC partitions. The reduction of hardware lowers the system cost and also improves the overall system reliability.

The issue of cost requires further clarification. In the current scheme, the LTCs and the local processors are part of the sub-detector readout system and sub-detectors are responsible for their purchase, installation and maintenance. In the proposed, centralised layout, the VME crates that accommodate all the TTC partitions are part of the CTP system and the CTP group becomes responsible for their purchase, installation and maintenance. This augments the actual cost of the CTP, but the CORE funding is sufficient to absorb the increase, especially since some saving will be made in the area of signal distribution. The quoted reduction (around 75%) refers to the *system as a whole*, affecting mainly the cost of sub-detector readout electronics.

Uniform interface

In contrast to the distributed scheme, the centralised layout would have a perfectly *uniform interface* to all the readout sub-detectors. This significantly simplifies the development, maintenance and upgrading of the readout, run-control and monitoring software.

Debugging and maintenance of the trigger system

All the sub-detector TTC partitions, wherever they will be located in the system, remain the responsibility of the CTP group. The initial testing and debugging, but even more so, the necessary maintenance, trouble-shooting and monitoring of the hardware during the lifetime of the experiment, will be significantly easier and more efficient in case of the centralised layout.

Stand-alone mode

The TTC partition (see section 2.2.1) enables the sub-detectors to operate in a *stand-alone* mode, at remote sites, or at times when the CTP is either not available or not required. Since the centralised scheme eliminates the LTCs, in order to run their system at remote sites, the sub-detectors will have to make use of their own VME crates and VME processors. They could continue to use the "private" crates and processors even when their electronics is installed in the experimental area, until they are ready to get integrated into the ALICE trigger system. At that point, their TTC partition will be transferred to the dedicated VME crates, close to the CTP (see **Figure 2**). The *stand-alone* mode of operation remains available with all the options it provides, but the control of the partition is now indirect - *via* the processor in the VME crate in which the TTC partition is located. The "transfer" and the "remote control" should not cause problems if proper provisions are made during the development of the necessary software, but, nevertheless, this could be seen as a possible disadvantage of the centralised layout.

Non-standard interface

Some ALICE sub-detectors are considering a development of a "custom" interface to the trigger system, to replace the "standard" TTC partition. Motivation usually comes from a small number of readout branches, low use of the LTC and the local VME processor, *etc*. . The intention is to keep the LTU and supplement it with a VME board that emulates the TTC part of the partition (TTCvi and TTCex boards). The board "extracts" all the trigger signals and transmits them, electrically, to the front-end electronics.

Although this "non-standard" approach remains possible in case of the centralised layout, it should be strongly discouraged:

- it takes significant effort to achieve a good hardware emulation, necessary to remain fully compliant with the control software;

- the "custom" interface complicates the system maintenance, even if the interface itself remains the responsibility of the sub-detector;
- the electrical connections to the sub-detector will be long, since the interface is located close to the CTP;
- the expected cost reduction could be negligible - the LTC and the local processor are no longer required.

A more constructive effort in saving time and money could be to organise a multi-sub-detector project, with the aim to develop a simple, common front-end interface, compatible with the standard TTC partition. The CTP group would offer every support to such an initiative.

2.4 Conclusion and plan of action

Taking into account the advantages and disadvantages discussed in the previous section, the CTP group believes that the *centralised layout*, as proposed in **Figure 2,** is a better overall solution, and *should be adopted for the ALICE trigger system*. The CTP group accepts to include the required VME crates and the VME processors as additional deliverables of the project, the increased project-cost being justified by a significant overall system saving.

The decision, as always, shall be made in consultation and with the agreement of the whole of ALICE collaboration. The purpose of this document is to start the process.

The choice of the trigger system layout affects the specification of the ALICE CTP as a whole, and the design of the LTU board in particular; it also affects, but to a lesser degree (the **BC** clock distribution, for example), the design of the sub-detector readout electronics. Both tasks are now in progress and, in order to avoid unnecessary delays, the decision on the final layout is *urgently* required

We hope that all the interested parties (sub-detector groups, project and system coordinators, *etc*.) will soon e-mail their comments. We believe that we could reach a decision during the workshop that is being planed for the beginning of April to deal with the other outstanding trigger issues (number of trigger inputs; the RoI option). The proposal would then be presented for approval at the following meeting of the ALICE Technical Board.