Timing issues - *a questionnaire*

Last updated: 10 July 2002

Introduction

The approved version of the *CTP User Requirement Document* (URD) makes no explicit demands on the *"quality"* of time-critical signals (**BC** clock, **L0** and **L1** trigger) - when the document was written, no reliable information about the timing requirements of sub-detectors was available and it was assumed that the issue would be assessed at a later data. The project is now entering a phase of conceptual design and the timing considerations strongly affect the key system decisions. Since a detailed and systematic survey of sub-detector requirement has not yet been completed, the following "questionnaire" shall attempt to provide the "early" information, necessary for future development work. *Sub-detectors' collaboration and prompt response will be highly appreciated.*

The issue is a delicate one: too tight tolerances complicate both the CTP hardware and the process of overall system time-tuning that involves the CTP *and also* the sub-detectors; unacceptably loose limits could have a detrimental effect on the performance; it is essential to find the right balance. In order to avoid misunderstandings and get the right answers, the questions are accompanied by lengthy explanations and comments - we thank in advance the sub-detector groups for their patience.

The three terms, frequently used in the text, have the following meaning:

LHC phase: the phase (± 12.5ns) of a clock or a signal *in respect to the LHC bunch crossing*; can only be evaluated indirectly.

Jitter: a cycle-to-cycle deviation of a clock or a signal edge from its average phase.

Drift: phase shift of a clock or a signal *in respect to the LHC bunch-crossing*, usually a long-term effect, caused by variations in temperature, power supply levels, changes of circuit propagation time, *etc.* ; likely to have a daily pattern.

The time-tuning of the system encompasses two processes - *synchronisation* and *alignment*. The *alignment* assures that all signals originating from the same bunch crossing reach the processing logic in the same clock cycle; it is achieved by delaying signals by an appropriate number of *full clock periods*. The *synchronisation* adjusts the phase of signal inputs to the local **BC** clock (and, indirectly, to the LHC bunch-crossing time); the synchronisation delays are *within one clock period* - 0 to 25ns. Although the synchronisation could affect the alignment - a delay could cause a signal to "slip" to the adjacent **BC** interval, ***this questionnaire deals only with the synchronisation issues*** and the consequences on alignment should not be considered.

The required "quality" of the BC clock

The **BC** clock in question is the clock transmitted *via* the TTC partition, derived from the TTCrx chip in the front-end electronics of the sub-detector. The usually quoted figure for the clock jitter is around 80ps (rms); it is the TTC system feature and, in *standard configuration*, no improvement is possible (it can get worse, on the other hand, if the design rules are not closely observed). In principle, the jitter is not affected by the overall system configuration.

If the quoted level of jitter is not acceptable for a particular sub-detector, alternative design approach must be considered. A clock with a jitter of around 10ps (rms) could be made available - an electrical output from the ALICE *TTC Machine Interface* (TTCmi). In that case, the handling and the distribution of the signal would be the sole responsibility of the sub-detector. We strongly advice to discuss the issue with the TTC guru, Bruce Taylor; you will certainly benefit from his knowledge of the system and his experience.

Question BC1

Is the 80ps (rms) jitter of the **BC** clock adequate for your application? If the answer is no, what is the level of jitter that your system can tolerate and how do you plan to achieve it?

The drift of the LHC phase of the **BC** clock, on the other hand, is dependant upon the overall system implementation. The schemes that have been considered require a similar level of hardware complexity, but offer different compromise between the simplicity of the time-tuning procedure and the inherent level of the LHC phase drift. The tasks of system tuning and its verification are not yet fully understood; it will be a (very) complex procedure, involving both the CTP *and* all the sub-detectors; it is likely to require the LHC beam and the readout data. Any simplification of the process would certainly benefit the system, but, before going too far, the required level of stability of the LHC phase of the **BC** clock (and the trigger signals) must be clearly understood.

Question BC2

Can your system, in normal working conditions, tolerate **±2ns** drift of the LHC phase of the **BC** clock? If the answer is no, what is the *maximum drift* you could cope with (that does not cause a relevant performance degradation)?

The initial LHC phase of the **BC** clock is completely unpredictable: just an additional couple of meters of electrical cable or the optical fibre produces a "dramatic" change; the phase (±12.5ns) cannot be directly measured. It is likely that, for most sub-detector, the setting of the phase, initial, or at any time, does not make any difference (compared to typical peaking time of 1.2µs, *etc.*). But there might be cases where a precise setting is essential and must be *adjusted* and *maintained* throughout the sub-detector operation.

Question BC3

Is the value of the LHC phase of the **BC** clock important for the operation of your sub-detector? If yes:

- How do you plan to tune the phase to the appropriate value?
- What is the required precision for the setting of the phase?

- Is the procedure a routine part of your setting/calibration and could it be performed when required and without major difficulties?
- Or, because of the difficulties, should the LHC phase of the **BC** clock, once set, never be changed (short of major modifications or mishaps)?

The timing of the L0 and L1 trigger signals

The latency of the **L0** trigger signal is one of the most critical parameters of the CTP system. The CTP URD sets the limit of 100ns for the signal generation, but any measure that could reduce the time even further is strongly encouraged. A number of options are being considered: the synchronisation of the last-arriving **L0** trigger input could be done by delaying the local CTP **BC** clock instead the signal itself; the **L0** trigger does not need to be re-synchronised with the LTU/TTC clock; *etc*. . The options affect, subtly but nevertheless, the timing of the **L0** trigger delivered to the front-end electronics and, before any design decision is made, the sub-detector requirements must be fully understood.

A brief reminder: the **L0** trigger shall be made available to sub-detectors as a differential LVDS signal; two parallel channels shall have connectors mounted on the LTU front panel; the signal distribution is a sole responsibility of sub-detectors.

Question L0

Is the LHC phase of the **L0** trigger sent to the front-end important for the operation of your sub-detector? If yes (see **Question BC3**):

- How do you plan to tune the phase to the appropriate value?
- What is the required precision for the setting of the phase?
- Is the procedure a routine part of your setting/calibration and could it be performed when required and without major difficulties?
- Or, because of the difficulties, should the LHC phase of the **L0** trigger, once set, never be changed (short of major modifications or mishaps)?

Another remainder: the **L1** trigger is sent to the sub-detectors via the TTC system; the signal is an output of the TTCrx chip, automatically synchronised with the local **BC** clock (another TTCrx output). The requirements set for the "quality" of the **BC** clock also define the timing characteristics of the **L1** signal. Please make sure that, in answering **Questions BC1**, **BC2** and **BC3,** you have taken into account the *effect of the properties of the local **BC** clock on the timing of the **L1** trigger.*

Again - a reminder: the time between the **L0** trigger and its corresponding **L1** decision is a programmable constant (a number of BC intervals); in case of a positive decision, the **L1** trigger is generated; the absence of the **L1** signal at the expected time indicates a negative decision ("L1 reject"). The duration of the **L0**-to-**L1** interval, seen by the sub-detector, could be affected by the timing properties of the local **BC** clock and the **L0** trigger. If permitted, in the worst case, the maximum variation shall not exceed 2 BC intervals (50ns). The sub-detector electronics should be able to tolerate that level of timing uncertainty, without any ill effect on the performance: the *Wait for **L1** Interval* should be extended by 2 BC periods; the

arrival of another **L0** trigger around (± 50ns) the expected time for **L1** should end the waiting and be interpreted as "L1 reject". Nevertheless, the unforeseen reasons might exist that would necessitate a more tight tolerance for the duration of the **L0**-to-**L1** interval. For that reason you are kindly asked to answer the following question.

Question L1

Can your system tolerate **±50ns** uncertainty in duration of the **L0**-to-**L1** interval (as seen by your front-end electronics)? If the answer is no, could you please briefly explain the reason and give the maximum tolerance you can cope with?

Many thanks for your effort and your patience!